SDC-RXV21

Floppy Controller Manual

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SDC-RXV21

Floppy Controller Manual

Sigma

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Section 1
General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the SDC-RXV21 floppy disc controller manufactured by Sigma Information Systems, Anaheim, California. The SDC-RXV21 supports one or two dual density, single or double sided floppy disc drives. The single dual-wide board is software and media compatible with DEC's* RXV21/RX02, and features an on-board bootstrap and diskette formatting capability.

The material in this manual is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief description of the SDC-RXV21, its logical track format, recording scheme, and a list of specifications.

Section 2 - INSTALLATION. This section explains the requirements and procedures for equipment installation. Alternate jumper selectable options and cabling are described.

Section 3 - OPERATION. This section explains the controller operation, including bootstrapping and formatting.

Section 4 - PROGRAMMING. A description of the SDC-RXV21 control registers and programming features is presented to aid the user in programming the controller.

*DEC, LSI-11, and Q bus are registered trademarks of Digital Equipment Corporation.

1.2 GENERAL DESCRIPTION

The SDC-RXV21 is a dual density floppy disc controller compatible with the DEC* RX01/RX02. When connected to a Shugart-type drive, it replaces the RXV21 subsystem. The controller provides either single density encoding compatible with IBM 3740 devices, or double density encoding. The controller provides 512K bytes of storage on a single diskette. When two floppy drives are used, each drive may operate at a different density.

The SDC-RXV21 is a single dual-wide board that plugs directly into any standard Q bus slot and interfaces through a 50-conductor ribbon cable to a Shugart compatible drive. The controller is factory preset for the standard device address 177170 and interrupt vector 264. The interrupt level is factory preset to level 4. Alternate addresses and interrupt vector are jumper selectable. Features include:

- Transparent firmware bootstrap which automatically boots double density diskettes (jumper selectable).
- Write precompensation to reduce bit shift for greater data integrity.
- Power fail protect to inhibit write sequence while the controller completes sector currently being written.
- Provides write current control for tracks greater than 43.
- Jumper selectable 4-level interrupt priorities compatible with LSI-11/23 or LSI-11/2.

1.3 COMPATIBILITY

The hardware, software and media compatibility with DEC's RXV21 system is provided to aid the user in data interchange with foreign systems.

HARDWARE. The controller is compatible with the LSI-11, LSI-11/2 and LSI-11/23 CPUs. The single dual-wide board plugs directly into any standard LSI-11 backplane. Alternate address selection and a 4-level device interrupt priority scheme that provides for expanded system configurations. Shugart 800/850-compatible drive logic is interfaced through a 50-pin ribbon connector.

SOFTWARE. The SDC-RXV21 is completely compatible with DEC's RXV21 register definition and command protocol. The SDC-RXV21 will operate, with no modification, with operating systems and diagnostics designed for the RX02.

MEDIA. Media (either preformatted or blank soft sectored diskettes) for the SDC-RXV21 is compatible with the IBM 3740. Recommended media are: IBM single or double density or DEC RX01/RX02.

1.4 LOGICAL TRACK FORMAT

Figure 1-1 defines each track format. The sector header field of each sector contains information describing both the sector and track number. All fields are recorded in FM except as noted in the following sections.

1.4.1 Sector Header Field

The header field consists of 7 bytes of information, preceded by a field of 6 bytes of "zero" data for synchronization.

Byte 1 ID ADDRESS MARK. A unique mark consisting of 1 byte of FE(hex) data with three missing clock-transitions using a C7 (hex) clock pattern. This mark is decoded by the controller and indicates the start of the sector header.

Byte 2 TRACK ADDRESS. This byte indicates the absolute ($0-114_8$) track address. Each sector contains this track information to locate its position on one of the 77 tracks.

Byte 3 "ZERO"

Byte 4 SECTOR ADDRESS. This byte indicates the absolute ($0-32_8$) sector address. Each sector contains this information to identify its position on the track.

Byte 5 "ZERO"

Byte 6,7 CRC. This is the 16-bit cyclic redundancy character and is calculated for each header from the first 5 bytes of information. Calculation, using the IBM 3740 polynomial, is defined in Section 1.4.3.

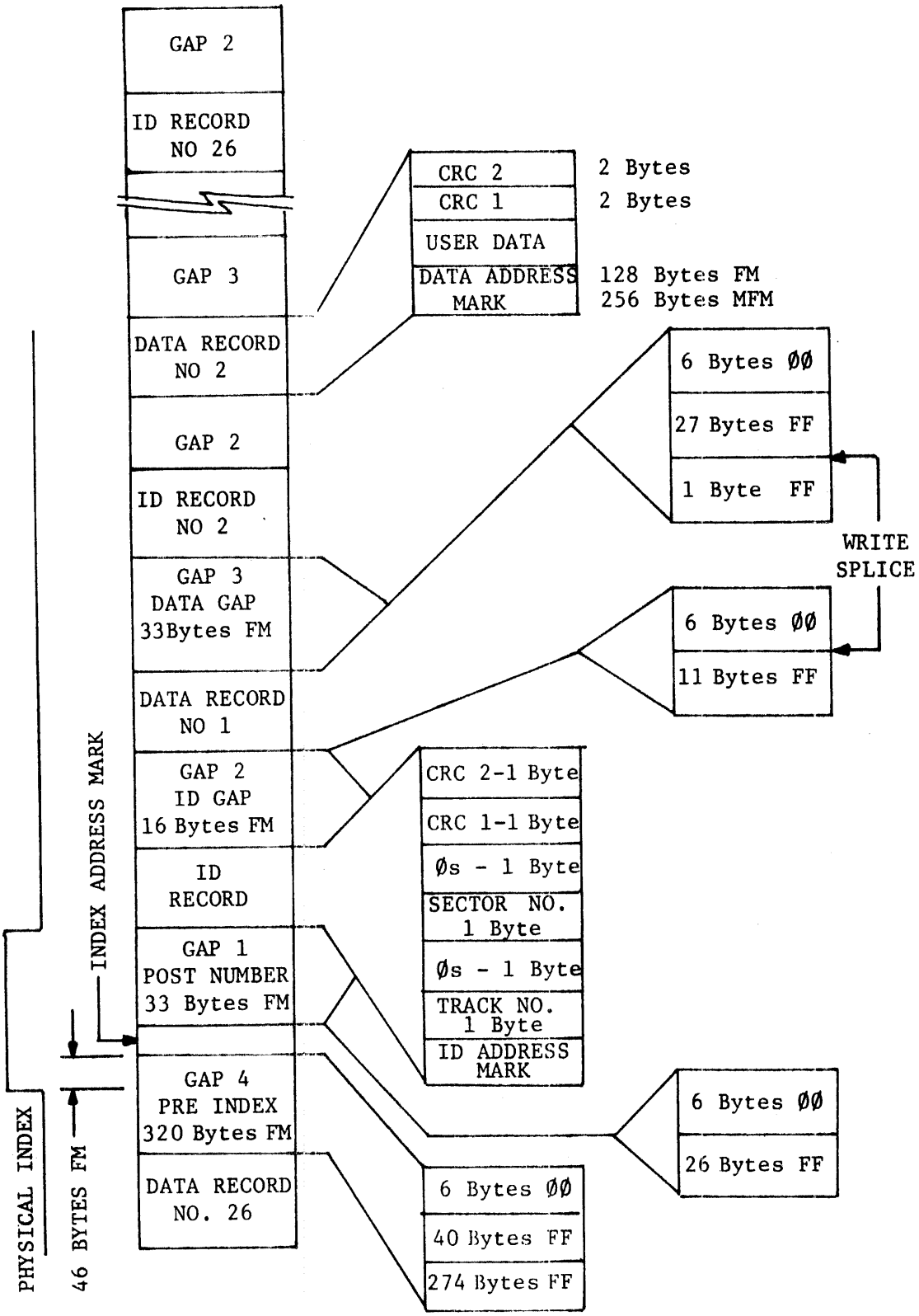


FIGURE 1-1: LOGICAL TRACK FORMAT

1.4.2 Data Field

The data field consists of either 131 or 259 bytes of information (depending on recording method), preceded by 6 bytes of "zero" data for synchronization.

The preamble and data address mark are written in FM. The user data and CRC character are written in either FM or modified MFM, depending on the formatted diskette density.

Byte 1 — DATA ADDRESS MARK. This byte is a unique mark consisting of a data byte with three missing clock transitions using a C7 (hex) clock pattern as defined in Table 1-1. This byte is written in FM and is decoded by the controller to indicate the start of the data field, FM vs MFM recording method, and deleted data field indication.

ADDRESS MARK	INDICATED DENSITY	DATA
INDEX	N/A	FC
ID	N/A	FE
DATA	FM	FB
	MFM Modified	FD
DELETED DATA	FM	F8
	MFM Modified	F9

TABLE 1-1: ADDRESS MARKS

Bytes 2-257 — FM (BYTES 2-129) OR MODIFIELD MFM (BYTES 2-257). This field is recorded in either FM or modified MFM. Either 128 or 256 bytes of information can be stored, depending on the encoding scheme.

Bytes 130-131 or 258-259 — CRC. This 16-bit cyclic redundancy character is calculated for each data field from the first 129 or 257 bytes of information using the IBM 3740 polynomial as defined in Section 1.4.3. These bytes are recorded with the same encoding scheme as the data field.

1.4.3 CRC - Cyclic Redundancy Check

Each sector header field and data field has a 2-byte (16-bit) CRC character which is the remainder that results when dividing the data bits [represented as a polynomial M(x)] by a generator polynomial G(x). The polynomial used for IBM 3740 is $G(x) = x^{16} + x^{12} + x^5 + 1$. Data bits include bytes 1-5 for the sector header, bytes 1-129 for an FM data field, and bytes 1-257 for an MFM data field.

1.5 RECORDING SCHEME

Double frequency (FM) and DEC modified Miller code (MFM) recording schemes are used by the SDC-RXV21. FM, used for single density recording, is compatible with IBM 3740 or DEC RX01 media. Modified MFM, used for recording double density, is compatible with the RX02 system.

1.6 SPECIFICATIONS

Power Requirements:	+5VDC at 2.5A (from LSI-11 backplane)
Bus Load:	1
Priority Level:	4-level compatible with LSI-11/23 CPU (Selectable alternates)
Device Address:	177170 (Selectable alternate at 177174)
Interrupt Vector:	264 (Selectable alternate at 270)
Interface:	Shugart compatible
Media:	RX01/RX02 compatible
Recording Method:	DEC modified MFM (Double density compatible RX02) or optional FM (single density compatible with IBM 3740)
Bootstrap:	On-board. Initiated when program execution starts at 173000. Can be disabled.
Cable:	Required standard 50-conductor 3M-type ribbon cable.
Temperature:	0°C to 45°C
Humidity:	10% to 95% non-condensing.

Section 2
Installation

2.1 CONTROLLER JUMPER CONFIGURATIONS

The SDC-RXV21 is shipped configured with DEC-standard operating parameters as defined in Table 2-1.

PARAMETER	SELECTION
Control Address	177170
Vector Address	264
Interrupt	Level 4
Firmware Bootstrap	Enabled
Write Precompensation	Enabled
Write Current Control	Disabled
Drive Select	Single or Double Sided

TABLE 2-1: FACTORY SET PARAMETERS

Most options are etched to the most often used operation. Etches must be cut before alternate jumpers are inserted. Several of the options are selectable by using AMP 530153-2 pin jumpers or, alternately, #30 wire wrap. Refer to Figure 2-1 for jumper locations.

NOTE: Certain jumpers are dedicated for factory test only. Jumpers 11-12, 13-14, 19-21 and 20-22 must NOT be removed. Jumper 17-18 must always be out.

2.1.1 Device and Vector Address Selection

The controller is shipped with the DEC standard device and vector addresses preset to 177170 and 264 respectively. Any change in these addresses requires a change in system software

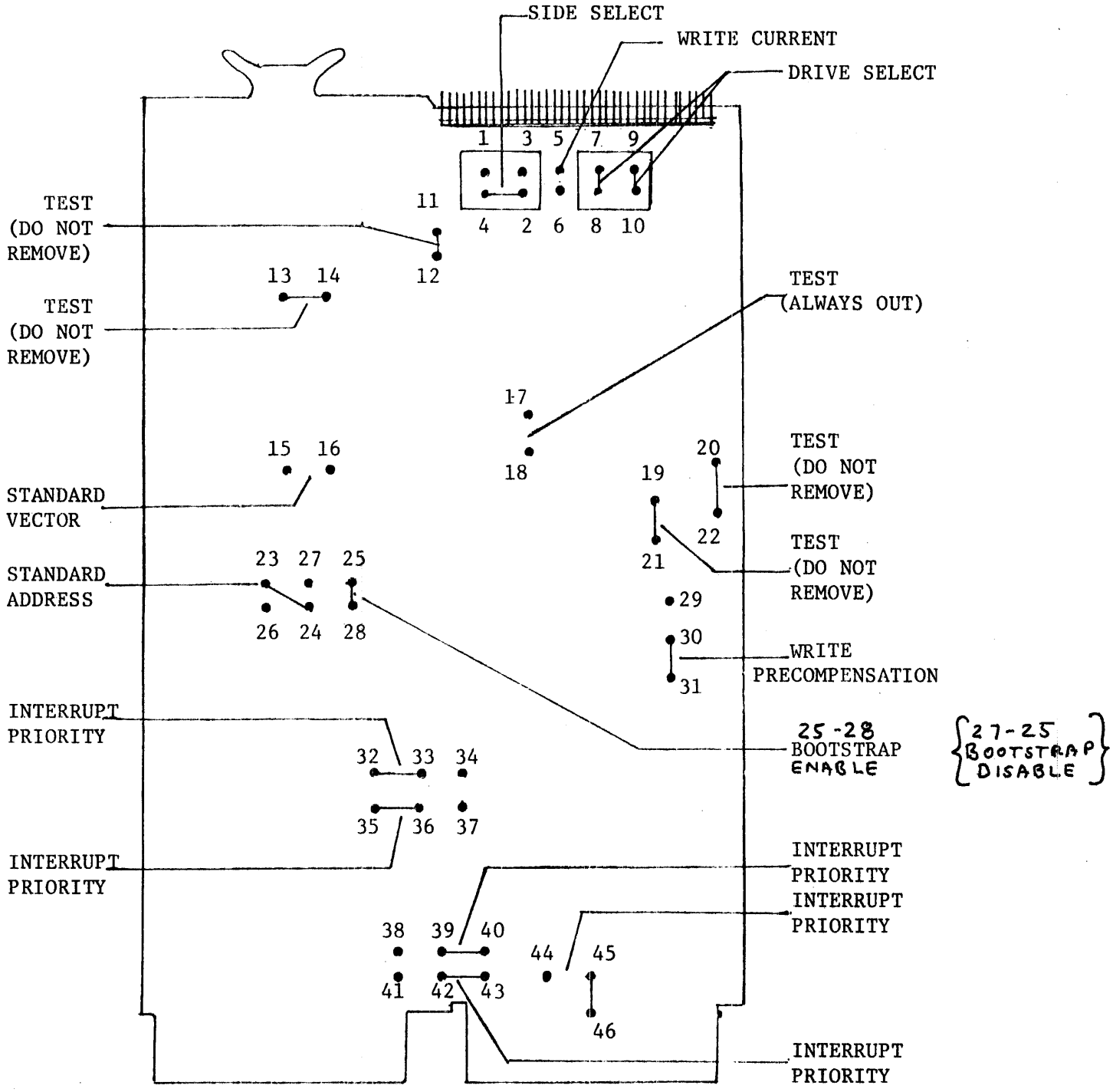


FIGURE 2-1: JUMPER LOCATIONS INDICATING FACTORY SET JUMPERS/ETCHES

The alternate device and vector addresses are selectable and are defined as 177174 and 270 respectively. These alternate addresses are typically used for systems with more than two drives where two controllers are required. To configure the second controller for address/vector assignments, cut the etch between W23 and W24; then jumper W24-W26 and W15-W16 as shown in Table 2-2.

OPTION	JUMPERS		
	23-24	24-26	15-16
Standard Device (177170) Vector (264) Addresses *	IN	OUT	OUT
Alternate Device (177174) Vector (270) Addresses	OUT	IN	IN

*Factory Preset

TABLE 2-2: DEVICE/VECTOR ADDRESS JUMPERS

2.1.2 Device Interrupt Priority

The SDC-RXV21 supports the 4-level device interrupt priority scheme compatible with the LSI-11/23. The controller asserts interrupt requests and monitors higher level request lines during interrupt arbitration The level 4 request is always asserted by the controller, regardless of its priority, to maintain compatibility with the LSI-11 and LSI-11/2 CPUs.

The interrupt priority is factory preset to level 4. If an alternate interrupt level is desired the following etches must be cut: W39-W40, W42-W43, W32-W33, W35-W36, and W45-W46. Refer to Table 2-3 for the jumper installation for the desired priority level.

PRIORITY LEVEL	ASSERT LEVEL	MONITOR LEVEL	JUMPERS									
			W32 W33	W33 W34	W35 W36	W36 W37	W38 W39	W39 W40	W41 W42	W42 W43	W44 W45	W45 W46
4*	4	5,6	IN	OUT	IN	OUT	OUT	IN	OUT	IN	OUT	IN
5	4,5	6	IN	OUT	OUT	IN	IN	OUT	OUT	IN	OUT	IN
6	4,6	7	OUT	IN	IN	OUT	OUT	IN	IN	OUT	IN	OUT
7	4,6,7	NONE	OUT	IN	OUT	IN	IN	OUT	IN	OUT	IN	OUT

*Factory Preset

TABLE 2-3: PRIORITY LEVEL CONFIGURATIONS

2.1.3 Bootstrap

The controller board contains a transparent firmware bootstrap which is initiated whenever program execution is started at location 173000, homing both drives to track Ø. Track 1, sector 1, of unit Ø is then read and diskette density is determined. For single density diskettes, sectors 1, 3, 5, and 7 are loaded into memory starting at location Ø. If the diskette is double density, sectors 1 and 3 are loaded. Program execution is then transferred to location Ø.

BOOTSTRAP	JUMPERS	
	W25-W28	W25-W27
Enable*	IN	OUT
Disable	OUT	IN

*Factory Jumpered

TABLE 2-4: BOOTSTRAP CONFIGURATIONS

NOTE: Only one bootstrap should be enabled in a system for proper operation. If a second bootstrap exists in the system, it must be disabled before enabling the SDC-RXV21 bootstrap.

2.1.4 Write Precompensation

The SDC-RXV21 controller provides hardware write precompensation to reduce bit shift. The RXV21 controller is shipped with write precompensation enabled. It is recommended that, for reliable operation, this feature not be disabled. However, if write precompensation must be disabled, remove the etch W30-W31 and insert jumper W29-W30 as shown in Table 2-5.

WRITE PRECOMPENSATION	JUMPERS	
	W29-W30	W30-W31
Enable*	OUT	IN
Disable	IN	OUT

*Factory Jumpered

TABLE 2-5: WRITE PRECOMPENSATION CONFIGURATIONS

2.1.5 Write Current Control

The SDC-RXV21 provides the necessary signal to reduce the write current for tracks greater than 43. This signal is available at pin 2 of the 50-pin ribbon connector.

Since single sided drives with Shugart-type 800 series interfaces do not require a write current signal, the controller is shipped with this feature disabled. However, double sided drives with Shugart-type 850 series interfaces do support write current control, and enabling this feature is recommended for double sided drives. This may be accomplished with jumper W5-W6 as shown in Table 2-6.

WRITE CURRENT	JUMPER W5-W6
Enable*	IN
Disable**	OUT

*Should be enabled for double sided drives

**Factory preset

TABLE: 2-6: WRITE CURRENT CONFIGURATIONS

2.1.6 Drive and Side Selection

The SDC-RXV21 controller has jumper options for both drive and side selection. Side select can be disabled, allowing operation on single sided drives only. The controller can be configured for either single or double sided drives. Jumpering allows one double sided drive to be addressed as two drives, where side Ø appears as drive Ø and side 1 appears as drive 1.

The controller, when shipped, is configured for either single or double sided drives. If double sided drives are used, it is recommended that write current control be enabled. Before selecting alternate options etch W2-W4 must be cut and then jumpers inserted as shown in Table 2-7.

DRIVE/SIDE SELECT	JUMPERS					
	W1-W2	W2-W3	W2-W4	W7-W8	W9-W10	W7-W9
Single Sided Drive	IN	OUT	OUT	IN	IN	OUT
Single or Double Sided Drive*	OUT	OUT	IN	IN	IN	OUT
Double Sided Drive Drive Ø = Side Ø Drive 1 = Side 1	OUT	IN	OUT	OUT	IN	IN

*Factory preset

TABLE 2-7: DRIVE/SIDE CONFIGURATIONS

2.2 DRIVE CONFIGURATIONS

For proper operation, the floppy drive(s) must be configured correctly. The controller uses radial drive selection and the drive(s) must be set up with this in mind. When two drives are used, the first drive is denoted Ø and the second drive 1. A particular drive is selected and remains selected after a function is complete, thus allowing the controller to poll drive status. A separate head load signal is provided by the control-er read and write functions on the diskette. The "in use" logic of the drive is configured as a function of head loading. Since the drives are homed without loading the heads during an initialize command, the drive is configured to provide stepper motor power independent of head loading. Refer to Table 2-8 for Shugart SA800/801, Table 2-9 for Shugart SA850/851, and Table 2-9 for Qume Data Trak 8 and YE-Data YD-174 strapping configurations.

DESCRIPTION	SHUGART JUMPER	DUAL DRIVES DRIVE Ø	DUAL DRIVES DRIVE 1	SINGLE DRIVE Ø
Drive Select 1	DS1	IN	OUT	IN
Drive Select 2	DS2	OUT	IN	OUT
Drive Select 3	DS3	OUT	OUT	OUT
Drive Select 4	DS4	OUT	OUT	OUT
Radial Head Loading Option	A	IN	IN	IN
Radial Head Loading Option	B	IN	IN	IN
Head Load Option	C	IN	IN	IN
In Use Option	D	OUT	OUT	OUT
Radial Head Loading Option	X	OUT	OUT	OUT
Inhibit Write When Protect	WP	IN	IN	IN
Allow Write When Protect	NP	OUT	OUT	OUT
Stepper Power from Drive Select	DS	IN	IN	IN
Stepper Power from Head Load	HL	OUT	OUT	OUT
In Use from Drive Select	Z	OUT	OUT	OUT
In Use from Head Load	Y	IN	IN	IN
Ready Output	R	IN	IN	IN
Index Output	I	IN	IN	IN
Disk Change Output	DC	X	X	X
Sector Output	S	X	X	X
Sector Option Disable	800	IN	IN	IN
Sector Option Enable	801	OUT	OUT	OUT
-5V DC Bias	L	IN	IN	IN
Termination HL	T1	OUT	IN	IN
Termination Drive Select	T2	IN	IN	IN
Termination Direction	T3	OUT	IN	IN
Termination Step	T4	OUT	IN	IN
Termination Write Data	T5	OUT	IN	IN
Termination Write Gate	T6	OUT	IN	IN

TABLE 2-8: CONFIGURATIONS FOR SHUGART SA800/801 INTERFACE DRIVES

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR Ø	DR 1	SINGLE DR Ø
SE	Termination for multiplexed standard input	IN	OUT	IN
DS1	Drive select 1 input pin	IN	OUT	IN
DS2	Drive select 2 input pin	OUT	IN	N/A
1B,2B,3B,4B	Side select option using drive select	OUT	OUT	OUT
RR	Radial ready	IN	IN	IN
RI	Radial index and sector	IN	IN	IN
R*	Option shunt for ready output	IN	IN	IN
2S	Two-sided status output	IN	IN	IN
850/51	Sector option enable	IN	IN	IN
I*	Index output	IN	IN	IN
S*	Sector output	OUT	OUT	OUT
DC	Disk change option	OUT	OUT	OUT
HL*	Stepper power from head load	OUT	OUT	OUT
DS	Stepper power from drive select	IN	IN	IN
WP	Inhibit write when write protected	IN	IN	IN
NP	Allow write when write protected	OUT	OUT	OUT
D	Alternate input - in use	OUT	OUT	OUT
M	Multi-media option	IN	IN	IN
DL	Door lock latch option	OUT	OUT	OUT
A,B*	Radial head load	IN	IN	IN
X*	Radial head load	OUT	OUT	OUT
C	Alternate input - head load	IN	IN	IN
Z*	In use from drive select	OUT	OUT	OUT
Y	In use from head load	IN	IN	IN
S1	Side select option using direction select	OUT	OUT	OUT
S2	Standard side select input	IN	IN	IN
S3	Side select option using drive select	OUT	OUT	OUT
TS,FS	Data separation option select	OUT	OUT	OUT
IW	Write current switch	IN	IN	IN
RS	Ready standard	IN	IN	IN
RM	Ready modified	OUT	OUT	OUT
HLL	Head load latch	OUT	OUT	OUT
IT	In use terminator	OUT	OUT	OUT
HI	Head load or in use to in use circuit	OUT	OUT	OUT
F	Remove for MFM encoding	OUT	OUT	OUT
AF	Install for FM or MFM encoding	IN	IN	IN
NF	Install for M2FM encoding	OUT	OUT	OUT
	*Shunt 4F			

TABLE 2-9: CONFIGURATIONS FOR SHUGART SA850/851 INTERFACE DRIVES

NOTE: For SA850/851 drives, a 16-pin programmable shunt, location 4F (P/N 15658), is provided for the eight most commonly used cut track options. These traces are usually shorted as shipped from the factory. The traces can be opened as follows:

Jumper Z	Open Pin 1 to Pin 16	Jumper HL	Open Pin 2 to Pin 15
Jumper A	Open Pin 3 to Pin 14	Jumper B	Open Pin 4 to Pin 13
Jumper X	Open Pin 5 to Pin 12	Jumper I	Open Pin 6 to Pin 11
Jumper R	Open Pin 7 to Pin 10	Jumper S	Open Pin 8 to Pin 9

DESCRIPTION	QUME JUMPER	DUAL DRIVES		SINGLE
		DRIVE Ø	DRIVE 1	DRIVE Ø
Drive Select 1	DS1	IN	OUT	IN
Drive Select 2	DS2	OUT	IN	OUT
Drive Select 3	DS3	OUT	OUT	OUT
Drive Select 4	DS4	OUT	OUT	OUT
Radial Head Load Option	A	IN	IN	IN
Radial Head Load Option	B	IN	IN	IN
Radial Head Load Option	X	OUT	OUT	OUT
In Use from Drive Select	Z	OUT	OUT	OUT
Stepper Power from Head Load	HL	OUT	OUT	OUT
Ready Alternate Output Pad	R	IN	IN	IN
Index Alternate Output Pad	I	IN	IN	IN
Alternate Input Head Load	C	IN	IN	IN
Alternate Input in Use	D	OUT	OUT	OUT
Alternate Output Disc Change	DC	IN	IN	IN
Alternate Output 2-Sided Disc Status	2S	IN	IN	IN
Stepper Power from Drive Select	DS	IN	IN	IN
In Use from Head Load	Y	IN	IN	IN
Door Lock Latch	DL	OUT	OUT	OUT
Radial Ready	RR	IN	IN	IN
Radial Index	RI	IN	IN	IN
Inhibit Write when Write Protected	HP	IN	IN	IN
Allow Write when Write Protected	NP	OUT	OUT	OUT
Drive Address, Select Pads (up to 8 Drives)	(D1, D2 / D4, DDS)	OUT	OUT	OUT
Two Headed Drive Select	(B1, B2 / B3, B4)	OUT	OUT	OUT
Head Select Option	S1	OUT	OUT	OUT
Head Select Option	S2	IN	IN	IN
Head Select Option	S3	OUT	OUT	OUT
Termination Resistor Pack	1TM	OUT	IN*	IN
Termination Resistor Pack	2TM	OUT	IN*	IN

*Termination resistor pack must be installed on drive 1 and removed from drive Ø on dual floppy systems. On single floppy systems, install the termination resistor on drive Ø.

TABLE 2-9: CONFIGURATIONS FOR QUME (DATA TRAK 8) AND VE-DATA (YD-174) INTERFACE DRIVES

2.3 CABLING

An optional 50-conductor ribbon cable connects the controller to a Shugart compatible drive. Connect the cable to the 50-pin connector located at the top of the controller board, observing the alignment of pin 1 as indicated in Figure 2-2. The cable can be purchased from an independent source, or the following list of materials (or equivalent) will aid in the construction of the required cable.

QTY	DESCRIPTION	MFG	P/N
1	50-pin controller connector	3M	3425-3000
2	50-pin drive connectors	3M	3415-0001
A/R	50 conductor ribbon cable	3M	3365/50

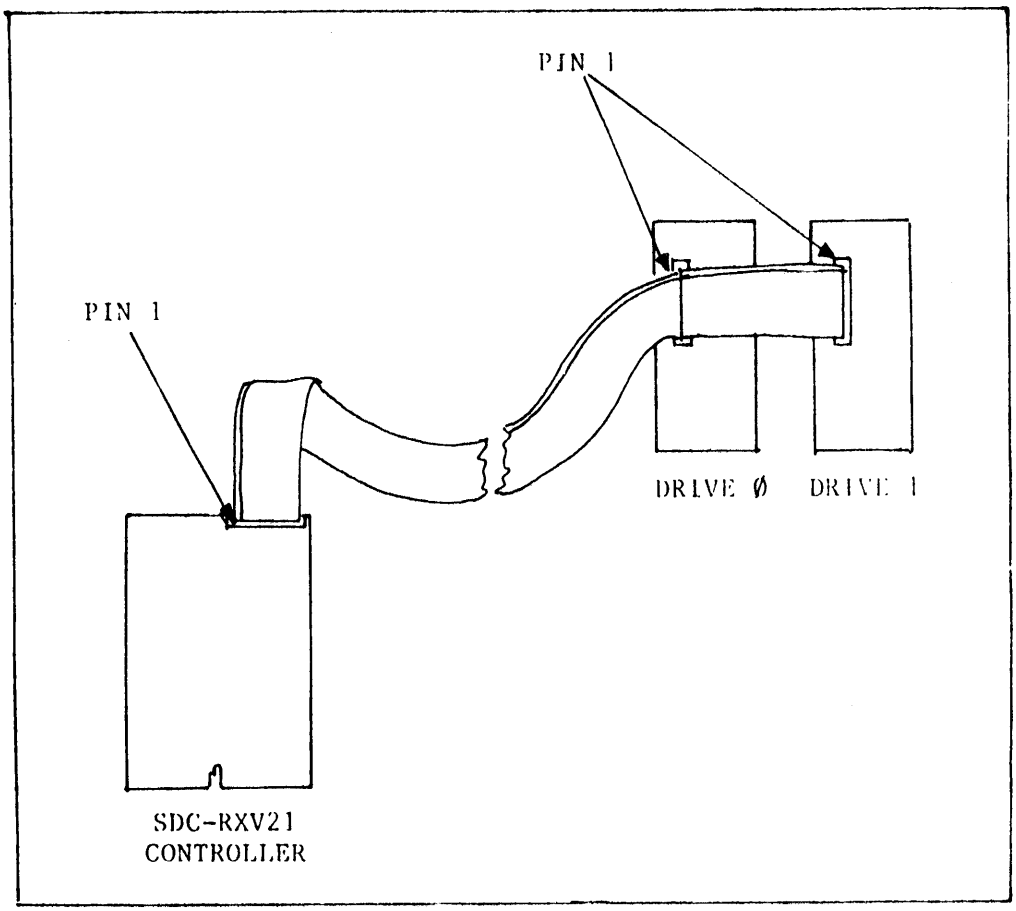


FIGURE 2-2: DRIVE/CONTROLLER CABLING

The connector pins illustrated in Figure 2-3 are compatible with Shugart-type 800/850 series interfaces.

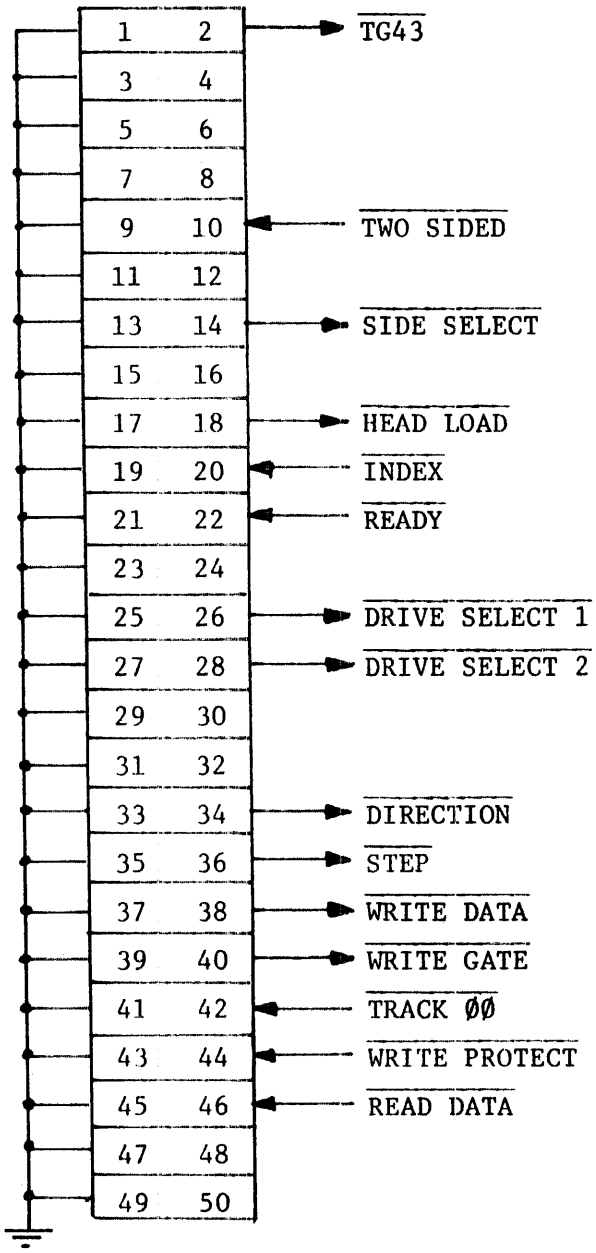


FIGURE 2-3: CONNECTOR PIN DEFINITIONS

2.4 CONTROLLER INSTALLATION

The SDC-RXV21 controller can be installed directly into any Q bus slot provided that interrupt and DMA continuity is maintained. These signals are daisy chained through the LSI-11 backplane and there should be no unused slots between the processor and the floppy controller. Priority sequences for the backplane can be found in the documentation accompanying the LSI-11 system. Note that when two interrupts of the same priority level are asserted, the device closer to the CPU receives the higher priority.

2.5 INITIAL CHECKOUT

After the controller jumpers and drive selection have been configured, initial checkout is performed using the following procedure.

NOTE

The bootstrap must be disabled
for the following procedure

1. Apply AC and DC power to the drive(s). The spindle should begin to rotate. The "in use" indicators on both drives should be off.

2. Place the RUN/HALT switch on the CPU to the HALT position and turn on the processor. An @ character on the terminal signifies that console ODT has been entered. First drive 1, then drive Ø, will step the heads inward 10 tracks; then step the heads outward until the home signal is detected. If heads will not load and/or "in-use" indicators do not light, check cabling and drive power supplies.

3. Place a preformatted scratch diskette in drive Ø.

4. If the standard address assignment is selected, open the Control Status (CS) register using ODT by typing 177170_8. The terminal will display 004040_8 the contents of the CS register. Deposit a 40000_8 in the CS by typing 40000 ⟨CR⟩. This command will initialize the controller. First drive 1, then drive Ø will calibrate for home position by stepping inward 10 tracks and then outward one track at a time until the drive indicates track Ø has been reached. After calibration the head on drive Ø is loaded. Sector 1 of track 1 is read into the controller buffer, as indicated by the in-use LED on drive Ø. The LED will remain on for a short time after the read operation is complete.

If, after initializing, the drives do not calibrate or the LED does not light, check the cabling and power supplies.

5. Reopen the CS (177170_8) using ODT as described above. The contents of this location should be 004040_8. Examine the next location (177172_8) by using the linefeed key or by typing 177172 ⟨CR⟩ which should yield either 204_8 or 244_8. For a detailed description of register protocol and bit definition, refer to Section 4.

6. Either diagnostics or an operating system can now be booted.

Section 3
Operation

3.1 GENERAL INFORMATION

This section provides the operating instructions for the SDC-RXV21 controller. Included are bootstrapping, formatting, fill/write, and read/empty operations. This sections also reviews operation with an RT-11 operating system.

3.2 BOOTSTRAPPING

If the bootstrap is enabled the SDC-RXV21 will respond to the standard bootstrap address 173000. The controller is booted by typing 173000G while in console ODT, causing a bus INIT and program execution transfer to 173000. An alternate method is to strap the LSI-11 CPU to power up in Mode 2, where on power-up, the CPU automatically starts execution at 173000. Power-up strapping procedures for the LSI-11 processor can be found in the Microcomputer Processors Handbook.*

To boot either a single or double density diskette, use the following procedure:

1. Place the diskette in drive Ø.

2. If the processor is stapped for power-up Mode 2, operating the INIT (boot) switch or cycle DC power OFF and ON.

3. If the processor is not strapped for power-up Mode 2 while in console ODT, type 173000G.

*Published by Digital Equipment Corporation, Maynard, MA, 1979.

3.3 FORMATTING

The SDC-RXV21 is capable of formatting diskettes in a specified density. The formatting is accomplished on two passes. During pass 1, an index address mark is written on tack Ø following the index hole. Twenty-six sector headers are written following the index address. Each of the remaining 76 tracks is written in the same manner. When track 76 is completed, pass 2 is initiated. The controller seeks track Ø and writes zero data field in sector 1 using the selected density. The remaining sectors are written in the same manner.

The format command selects diskette density, unit and side (for dual drives). Table 3-1 defines the command words.

DENSITY/SIDE	UNIT Ø	UNIT 1
Single Density Side Ø	11	31
Single Density Side 1	1011	1031
Double Density Side Ø	411	431
Double Density Side 1	1411	1431

TABLE 3-1: DENSITY/SIDE COMMANDS

Figure 3-1 illustrates a format subroutine. The format command is loaded into RXVCS. When TRAN REQ is set, the keyword 222 is loaded into RXVDB. When the diskette is formatted a return is made.

```
FORMAT:

        MOV #11, CMD            ;FORMAT
        BIS DENS, CMD           ;DENSITY
        BIS UNIT, CMD           ;UNIT
        BIS SIDE, CMD           ;SIDE
        MOV CMD, @#RXVCS        ;SELECT FUNCTION
        JSR PC, TRWAIT          ;WAIT FOR TR
        MOV #222, @#RXVDB       ;KEYWORD
        JSR PC,DNWAIT           ;WAIT FOR DONE
        TST @#RXVCS             ;ERROR
        BMI FRMERR              ;BR IF SO
        RTS PC

FRMERR:
```

FIGURE 3-1: FORMAT SUBROUTINE

Alternately, a diskette can be formatted using console ODT. Open the Control and Status (CS) register and deposit the appropriate command. Then deposit the format key word, 222, in the Data Buffer (DB) register. The following is an example of formatting unit Ø side Ø in double density:

```
177170      004040    411 <LF>
177172      000000    222 <CR>
```

3.4 FILL/WRITE OPERATION

Figure 3-2 illustrates subroutines to write data on a diskette. This is done by performing a Fill Buffer operation followed by a Write Sector operation.

```
FILLBF:

   MOV     #1, CMD              ;FILL BUFFER
   BIS     DENS, CMD            ;DENSITY
   MOV     CMD, @#RXVCS         ;SELECT FUNCTION
   JSR     PC TRWAIT            ;WAIT FOR TR
   MOV     COUNT, @#RXVDB       ;WORD COUNT
   JSR     PC, TRWAIT           ;WAIT FOR TR
   MOV     #BUFOUT, @#RXVDB     ;BUS ADDRESS OF DATA
   JSR     PC, DNWAIT           ;WAIT FOR DONE
   TST     @#RXVCS              ;ERROR
   BMI     ERFIL                ;BR IF SO
   RTS     PC

ERFIL:

WSECT:

   MOV     #5, CMD              ;WRITE, SECTOR
   BIS     DENS, CMD            ;DENSITY
   BIS     UNIT, CMD            ;UNIT
   BIS     SIDE, CMD            ;SIDE
   MOV     CMD,@#RXVCS          ;SELECT FUNCTION
   JSR     PC, TRWAIT           ;WAIT FOR TR
   MOV     SECTOR, @#RXVDB      ;SECTOR
   JSR     PC TRWAIT            ;WAIT FOR TR
   MOV     TRACK @#RXVDB        ;TRACK
   JSR     PC, DNWAIT           ;WAIT FOR DONE
   TST     @#RXVCS              ;ERROR
   BMI     WSERR                ;BR IF SO
   RTS     PC

WSERR:
```

FIGURE 3-2: WRITE DATA SUBROUTINES

3.5 READ/EMPTY OPERATIONS

Figure 3-3 describes subroutines to read data from a diskette. This is done by performing a Read Sector operation, followed by an Empty Buffer operation.

```
RSECT:

   MOV    #7, CMD              ;READ SECTOR
   BIS    DENS, CMD            ;DENSITY
   BIS    UNIT, CMD            ;UNIT
   BIS    SIDE, CMD            ;SIDE
   MOV    CMD, @#RXVCS         ;SELECT FUNCTION
   JSR    PC, TRWAIT           ;WAIT FOR TR
   MOV    SECTOR, @#RXVDB      ;SECTOR
   JSR    PC, TRWAIT           ;WAIT FOR TR
   MOV    TRACK, @#RXVDB       ;TRACK
   JSR    PC, DNWAIT           ;WAIT FOR DONE
   TST    @#RXVCS              ;ERROR
   BMI    RSERRR               ;BR IF SO
   RTS    PC

RSERR:

EMPBF:

   MOV    #3, CMD              ;EMPTY BUFFER
   BIS    DENS, CMD            ;DENSITY
   MOV    CMD, @#RXVCS         ;SELECT FUNCTION
   JSR    PC, TRWAIT           ;WAIT FOR TR
   MOV    COUNT, @#RXVDB       ;WORD COUNT
   JSR    PC, TRWAIT           ;WAIT FOR TR
   MOV    #BUFFIN, @#RXVDB     ;BUS ADDRESS FOR DATA
   JSR    PC, DNWAIT           ;WAIT FOR DONE
   TST    @#RXVCS              ;ERROR
   BMI    EREMP                ;BR IS SO
   RTS    PC

EREMP:
```

FIGURE 3-3: READ DATA SUBROUTINES

3.6 OPERATION USING RT-11

The SDC-RXV21 controller requires a different handler than the single density controllers. This handler is configured to use the DMA transfer scheme of the controller. Also, diskette density is determined by the handler without system intervention, allowing the use of either single or double density diskettes interchangeably.

This handler, designated "DY," is available in RT11-V03B and later revisions.

3.6.1 Creating a DY-Compatible System Disk

Use the following procedure to create a DY-based system.

Using an RX01 (or equivalent) system, or a system which has an RX01 (or equivalent) peripheral device, copy the monitor file and other associated system files onto a single density diskette. These files can be obtained from the binary distribution media or by performing a SYSGEN and specifying DY as the system device. The following commands will initialize the diskette and copy the necessary files to Drive 1.:

```
.INIT/NOQUERY DX1:
.COPY/SYS SYS: SWAP.SYS DX1:
.COPY/SYS SYS: DYMNXX.SYS DX1:
.COPY/SYS SYS: TT.SYS DX1:
.COPY/SYS: DIR.SAV DX1:
.COPY SYS: PIP.SAV DX1:
.COPY SYS: DUP.SAV DX1:
```

The bootstrap must then be copies from the monitor file to block ϕ of the diskette. The following command will accomplish this on the diskette in drive 1.

```
.COPY/BOOT DX1: DYMNXX DX1:
```

This diskette can be used with the SDC-RXV21 controller but it is single density. To build a double density diskette, first format a diskette to double density as explained in Section 3.3. Boot the single density system diskette in drive Ø. Use the following commands to initialize the formatted diskette in drive 1 and copy the system software from drive Ø to drive 1.

```
.INIT/NOQUERY DY1:
.COPY/SYS DY:*.* DY1:
```

Finally, copy the bootstrap to block Ø of the diskette in drive 1.

```
.COPY/BOOT DY1: DYMNXX DY1:
```

The diskette in drive 1 can now be booted as a double density diskette.

Section 4
Programming

4.1 GENERAL INFORMATION

This section defines device registers and command protocol for the SDC-RXV21.

Software control of the SDC-RXV21 is performed by means of two device registers: the Command and Status (RXVCS) register and a multipurpose Data Buffer (RXVDB) register with addresses 177170 and 177172 respectively. With few exceptions, the registers can be read or write using instructions referring to their addresses.

The RXVCS passes control information from the CPU to the controller and reports status and error information from the controller to the CPU. The RXVDB provides additional control and status information between the CPU and the controller. Information in the RXVDB is a function of the controller operation in progress.

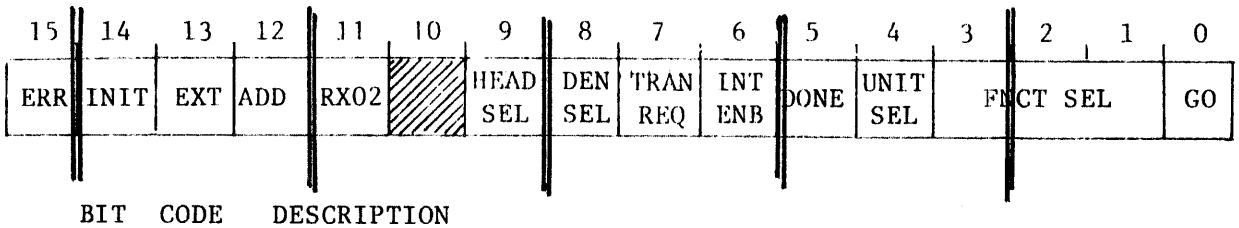
The controller contains a sector buffer capable of storing a complete sector. For Read/Write operations the buffer is either filled before a Write command or emptied after a Read command under DMA control. During a Read the desired sector is located and the sector data are transferred to the buffer.

A detailed description of bit assignments are given for registers:

Command and Status	RXVCS	177170
Data Buffer	RXVDB	
Track Address	RXVTA	
Sector Address	RXVSA	177172
Word Count	RXVWC	
Bus Address	RXVBA	
Error and Status	RXVES	

4.2 COMMAND AND STATUS REGISTER - RXVCS (177170)

Functions are initiated by loading the Command and Status register, when not busy (bit 5 = 1), with bit 0 = 1.



BIT	CODE	DESCRIPTION
15	ERR	ERROR. This bit is set by the controller if an error occurs during an attempt to execute a command. Cleared by INIT or the initiation of a new command. When an error is detected the RXVCS is read into the RXVDB. Read Only.
14	INIT	INITIALIZE. This bit, set by the program, initializes the controller without initializing all the devices on the LSI-11 bus. Write Only.

CAUTION

Loading the lower byte of the RXVCS will also load the upper byte of the RXVCS.

When set, the controller will negate DONE and move the head position mechanism of drive 1 (if two drives are available) to track Ø. When completed, the controller will repeat the operation on drive Ø. The controller then clears the Error and Status register, sets Initialize Done, and Drive Ready if drive Ø is ready. Finally the controller reads sector 1, track 1, of drive Ø.

12 13	EXT ADD	EXTENDED ADDRESS. These bits define an extended bus address, bit 12 = MA16, Bit 13 = MA17. Write Only.
11	RX02	RX02. This bit, asserted by the controller, indicates an RX02-type system. Read Only.
10		NOT USED. Must be written as a zero.
9	HEAD SEL	HEAD SELECT. This bit determines the side of the disc for execution of the desired function: bit cleared = side Ø, bit set = side 1. Read/Write.

8	DEN SEL	DENSITY SELECT. This bit defines either single or double density operation. Bit cleared = single density, bit set = double density. Read/Write.
7	TRAN REQ	TRANSFER REQUEST. This bit indicates the controller needs data or has data available. Read Only.
6	INT ENB	INTERRUPT ENABLE. This bit, set by the program, enables an interrupt when the controller completes an operation and asserts DONE. Cleared by INIT. Read/Write.
5	DONE	DONE. This bit indicates the completion of a function. It generates an interrupt when asserted if INT ENB is set. Read Only.
4	UNIT SEL	UNIT SELECT. This bit selects one of two discs for execution of the desired function. Read/Write.
3-1	FNCT SEL	These bits define one of eight operations listed below and described in detail in Section 4.3.

ØØØ Fill Buffer
ØØ1 Empty Buffer
Ø1Ø Write Sector
Ø11 Read Sector
1ØØ Set Media Density/Format
1Ø1 Read Status
11Ø Write Deleted Data Sector
111 Read Error Code

0	GO	GO. Initiates a command to the controller. Write Only.

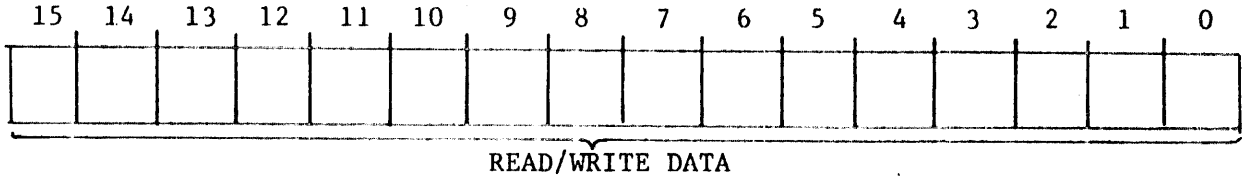
4.3 DATA BUFFER (177172)

This register is a general purpose data path between the SDC-RXV21 and the LSI-11. It represents one of six registers (RXVDB, RXVTA, RXVSA, RXVWC, RXVBA, and RXVES). These registers are addressable only under the protocal of the function in progress.

This register is Read/Write if the controller is not in the process of executing a command (i.e., it may be manipulated without affecting the controller). When the controller is executing a command, this register is Read/Write only if RXVCS, bit 7 (TRAN REQ) is set.

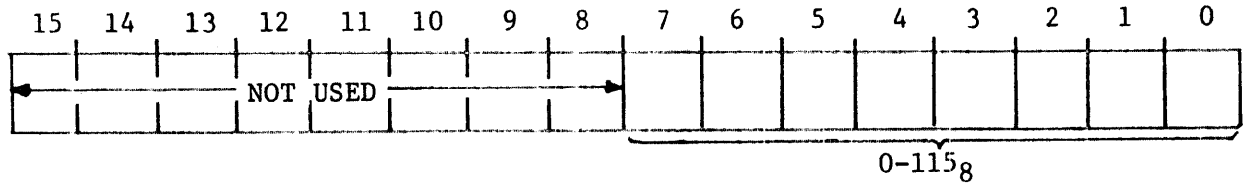
4.3.1 Data Buffer Register (RXVDB)

All information transferred to and from the floppy media passes through the RXVDB register.



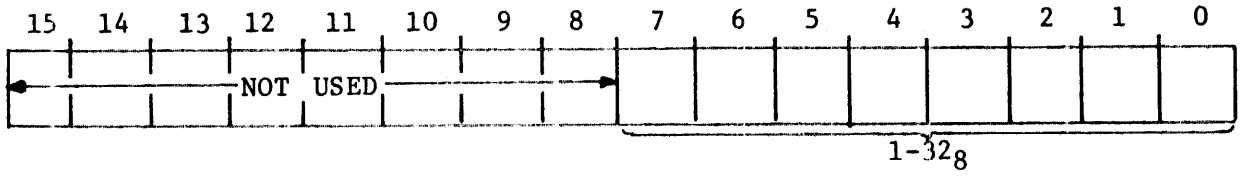
4.3.2 Track Address Register (RXVTA)

This register is loaded to indicate on which of the 115_8 (77_{10}) tracks a given function operates.



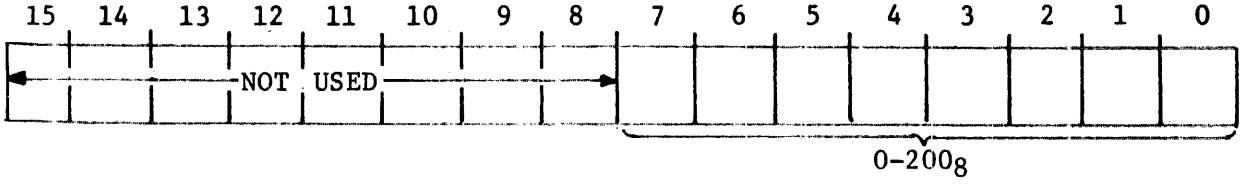
4.3.3 Sector Address Register (RXVSA)

This register is loaded to indicate on which of the 32_8 (26_{10}) sectors a given function operates.



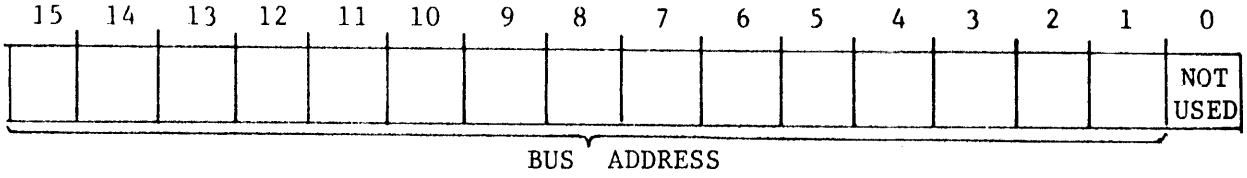
4.3.4 Word Count Register (RXVWC)

This 8-bit register is loaded with the number of words (128_{10} maximum) to be transferred. At the end of each transfer the Word Count register is decremented. When the contents of RXVWC are decremented to zero, transfers are terminated, DONE is set (RXVES, bit 5), and, if enabled, an interrupt is requested. If the word count is greater than the limit for the density specified, the controller asserts WC OVFL (RXVES bit 10).



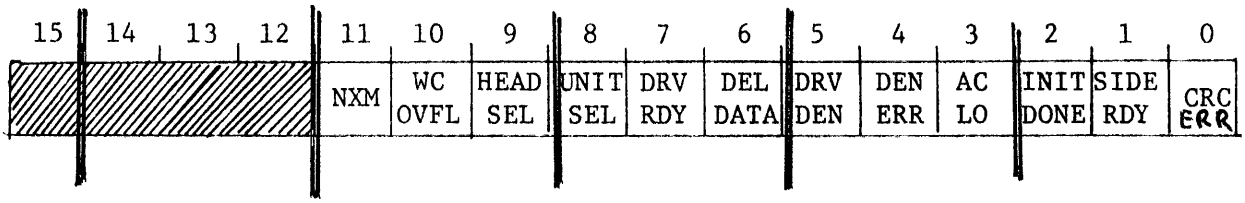
4.3.5 Bus Address Register (RXVBA)

This register is used to generate the bus address, defining the location of data transfer. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the Control and Status register. Systems with only 16 address bits will wraparound to location zero when the extended address bits are incremented.



4.3.6 Error and Status Register (RXVES)

This register contains the current error and status conditions of the drive selected by bit 4, Unit Select, of the RXVCS. The RXVES is loaded into the RXVDB upon completion of a function. Read Only.



15-12		NOT USED.
11	NXM	NONEXISTENT MEMORY ERROR. This bit is asserted by the controller when the memory address specified for a DMA operation is nonexistent.
10	WC OVFL	WORD COUNT OVERFLOW. This bit indicates that the specified word count is greater than the limit for the density selected. When this error is detected the controller terminates the fill or empty buffer operation and asserts the Error and Done bits.
9	HEAD SEL	HEAD SELECT. This bit indicates the selected side. Bit cleared = side Ø, bit set = side 1.
8	UNIT SEL	UNIT SELECT. This bit indicates the selected drive. Bit cleared = drive Ø, bit set = drive 1.

7	DRV RDY	DRIVE READY. This bit is asserted if the selected drive exists with proper power, a diskette installed, door closed, and a diskette up to speed. This bit is valid when retrieved via a Read Status function or at the completion of INIT, when it indicates the status of drive Ø.
6	DEL DATA	DELETED DATA. This bit indicates that, during data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
5	DRV DEN	DRIVE DENSITY. This bit indicates the density of the diskette in the selected drive. Bit cleared = single density, bit set = double density.
4	DEN ERR	DENSITY ERROR. This bit indicates a density error was detected when information was retrieved from the data field of the diskette. A density error occurs when the density selected differes from that of the data field. Upon detecting this error the controller loads the RXVES into the RXVDB and asserts the Error andDone bits.
3	AC LO	ACLO. This bit, set by the controllers, indicates a power failure.
2	INIT DONE	INITIALIZE DONE. This bit indicates completion of the initialize routine, which can be caused by system power failure or by programmable LSI-11 bus initialize.
1	SIDE RDY	SIDE READY. This bit is asserted by the controller when a double sided drive is selected, is ready, and has double sided media inserted. When asserted, this bit indicates that side 1 of the selected drive is available for Read and Write operations.
0	CRC	CRC ERROR. This bit indicates a cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The information stored in the buffer becomes invalid. Upon detection of this error the controller loads the RXVES into the RXVDB and asserts the Error andDone bits.

4.4 EXTENDED STATUS REGISTERS

The SDC-RXV21 controller has four internal status registers. These registers provide error information and drive status informtion. The registers can be retrieved by a read error code function as described in Section 4.8.8.

4.4.1 Word 1 ⟨7:0⟩ - Definitive Error Code

OCTAL	ERROR CODE DESCRIPTION
Ø4Ø	Attempt to access a track greater than 76.
Ø5Ø	Home found before desired track was reached.
Ø7Ø	Desired sector not found after investigating 52 headers (2 revolutions).
12Ø	Preamble not found.
15Ø	Header track address of a good header not comparable with the desired track.
16Ø	Too many tries for an IDAM (identifies header).
17Ø	Data AM not found in alloted time.
2ØØ	CRC error on reading the secotr from the disc.
24Ø	Density Error
25Ø	Wrong key word for Set Media Density command.
26Ø	Illegal Data AM.
27Ø	Invalid POK during write sequence.
3ØØ	Drive not ready.
31Ø	Drive write protected.

4.4.2 Word 1 ⟨15:8⟩ - Not Used

This register is always cleared by the controller.

4.4.3 Word 2 ⟨7:0⟩ - Current Track Address of Drive Ø

This register (cleared during INIT to synchronize with actual track position) is updated with each Seek on drive Ø and maintains current track position.

4.4.4 Word 2 ⟨15:8⟩ - Current Track Address of Drive 1

This register (cleared during INIT to synchronize with actual track position) is updated with each Seek on drive 1 and maintains current track position.

4.4.5 Word 3 ⟨7:0⟩ - Target Track of Current Disc Access

If legal, the track specified for the last Read/Write command is saved in this register.

4.4.6 Word 3 ⟨15:0⟩ - Target Sector of Current Disc Access

The sector specified for the last Read/Write command is saved in this register.

4.4.7 Word 4 ⟨15:8⟩ - Track Address of Selected Drive

This register contains the track address read from the sector header of the desired sector during the last Read/Write command.

4.5 COMMAND PROTOCOL

Data storage and recovery using the SDC-RXV21 controller is accomplished by manipulation of the Control and Status (RXVCS) and Data Buffer (RXVDB) registers according to the protocol of the individual functions. The penalty for violation of protocol can be permannent loss of data. Each of the functions are encoded and written into the RXVCS, bits 1-3, as described in Section 4.2. The detailed protocol for each function is described below.

4.5.1 Fill Buffer (ØØØ)

This function is used to fill the controller buffer with data from the host CPU. The host specified the number of words to be transferred. The command density bit determines the buffer size (64 or 128 words). The controller zero-fills the remaining buffer space. If the word count is too large for the density selected, the function is aborted, Error and Done are asserted and the Word Count Overflow bit is set in the RXVES.

The contents of the buffer may be written on the diskette with a subsequent Write Sector command, or returned to the host CPU using an Empty Buffer command.

When the command is loaded, RXVCS, bit 5 (DONE) is negated. RXVCS, bit 8, (DEN) must be set to define the buffer size. RXVCS, bits 12 and 13 (Extended Address) must also be asserted to define the extended memory segment used with the buffer address yet to be specified, to form the absolute memory address of the data to be transferred. RXVCS, bit 4 (UNIT SEL) and bit 9 (HEAD SEL) are ignored since no drive operation is required. When RXVCS, bit 7 (TRAN REQ) is first asserted, the program must move the word count into the RXVDB, which will negate TRAN REQ.

When the controller again asserts TRAN REQ, the program must move the buffer address into the RXVDB. The controller then negates TRAN REQ, initiates a DMA cycle, and transfers the first word from the host to the controller buffer. At the end of the transfer the Word Count register is decremented and the buffer address is incremented by two. This cycle is repeated until the Word Count register becomes zero. The controller zero-fills the remaining buffer space, set the DONE bit, and if enabled, causes an Interrupt Request. After DONE is asserted the RXVES is moved into the RXVDB.

During the data transaction, if any non-existent memory is addressed, the controller will time out and abort the function. The ERR and DONE bits will be asserted. RXVES, bit 11 (NXM) will be set the the RXVES will be moved into the RXVDB. If enabled, an Interrupt Request will be generated.

4.5.2 Empty Buffer (ØØ1)

This operation transfers the contents of the controller to the host CPU which specifies the number of words to be transferred. The command density bit determines the maximum legal word count. If the word count specified is too large for the density selected, the function is aborted, ERR and DONE are asserted and the Word Count Overflow (WC OVFL) is set in the RXVES.

The contents of the buffer may be transferred to the host as many times as desired or may be written on the diskette with a subsequent Write Sector command. Unless a Fill Buffer or Read Sector command is issued, the controller buffer is not destroyed.

When the command is loaded, RXVCS bit 5 (DONE) is negated, and bit 8 (DEN SEL) must be set to allow the proper word count limit. Bits 12 and 13 (EXT ADD) must also be asserted to define the extended memory segment used with the buffer address (yet to be specified) to form the absolute memory destination address. Bit 4 (UNIT SEL) and bit 9 (HEAD SEL) are ignored since no drive operation is required. When bit 7 (TRAN REQ) is first asserted the program moves the word count into the RXVDB, which negates TRAN REQ. When TRAN REQ is again asserted the program moves the buffer address into the RXVDB. The controller then negates TRAN REQ, initiates a DMA, and transfers the first word of the buffer to the host. At the end of the transfer, the Word Count register is decremented and the Buffer Address register is incremented by two. This cycle is repeated until the Word Count register becomes zero.*

During DMA transactions, if any non-existent memory is addressed, the controller will time-out and abort the function. An ERR bit will be asserted.*

4.5.3 Write Sector (Ø1Ø)

The Write Sector function locates a desired track and sector, and writes the sector with the contents of the internal sector buffer. When RXVCS is loaded with this command, the RXVES is cleared and TRAN REQ and DONE are negated. When TRAN REQ is first asserted, the program loads the desired sector address into the RXVDB, which negates TRAN REQ. When TRAN REQ is again asserted the program loads the desired track address into the RXVDB, which negates TRAN REQ. The controller then seeks the desired track and sector. The desired track and track field of the sector header are compared. If they do not match the operation is aborted and ERR is asserted.*

*DONE is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request will be generated at this point.

If the densities agree but the desired sector cannot be located within two revolutions, the operation will be aborted and ERR will be asserted.*

If the desired track and sector are located and the densities agree, the contents of the internal sector buffer are written, followed by a CRC character in the selected density.* NOTE: The contents of the sector buffer are not destroyed by a Write Sector operation.

CAUTION

> The contents of the internal sector buffer are lost during a power failure. However, after power is recovered, a Write Sector command will cause the random contents of the buffer to be written on the diskette with a valid CRC character.

4.5.4 Read Sector (Ø11)

This function locates the desired track and sector and transfers the contents of the data field into the internal sector buffer. When the RXVCS is loaded with this command, the RXVES is cleared and the TRAN REQ and DONE bits are negated. When TRAN REQ is first asserted the program loads the desired sector address into the RXVDB, which will negate TRAN REQ. When TRAN REQ is again asserted the program loads the desired track address into the RXVDB, which will negate TRAN REQ.

TRAN REQ and DONE bits remain negated while the desired sector is located. If after two revolutions the desired sector is not located the operation is aborted, and ERR is asserted.

When the desired sector is located, the desired track and the track field of the sector header are compared. If they do not agree, the operation is aborted and ERR is asserted.

If the desired track and sector agree, the data address mark is read and diskette density is determined. If the diskette density does not compare with the function density, the operation is aborted and ERR is asserted.

If a legal data address mark is located and the densities of the diskette and function agree, data from the sector is read into the internal buffer. If the data address mark indicates a deleted data field, RXVES bit 6 (DEL DATA) is set. As data are stored in the internal buffer a CRC is computed and the CRC bytes are recorded. A non-zero

*DONE is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request will be generated at this point.

result indicates a Read Error. When a CRC error is encountered, RXVES bit Ø (CRC) is set.*

If the desired sector is located, the density of the diskette and the function agree, and the data are transferred with no CRC error, DONE is asserted and, if enabled, an Interrupt Request will be generated.

4.5.5 Set Media Density (1ØØ)

This dual purpose function can set media density or "reformat" a diskette. Media density is set by reqriting all the data address marks (single or double density) and writing zero data fields in the selected density. "Reformatting" the entire diskette is done by writing both the sector headers and the data fields. The data fields are written in the selected density preceded by the corresponding data address mark. Both commands are initiated by the Set Media function but differ in the keyword required to execute the command.

When the RXVCS is loaded with Set Media Density, the RXVES is cleared and DONE is negated. When TRAN REQ is set the program responds with a keyword which must be deposited in the RXVDB to complete the protocol. When the controller recognizes this character, it begins executing the command. If an illegal keyword is used, the operation is aborted.*

If the keyword is 111, a Set Media Density operation is asserted. This operation starts at track Ø, sector 1. Each sector header is located and a Write operation is initiated. A data field is written with zero data in the selected density. If an error occurs while reading any header, the operation is aborted.* If the operation is successfully completed, DONE is set and, if enabled, the controller asserts an Interrupt Request.

If the keyword is 222, a Format operation is initiated. This function starts at the physical index of track Ø. Each track is written first with an index address mark, then 26 sector headers are written sequentially about the track. When each track is written Set Media Density is set as described above.

The following input string will format the selected unit, in the desired density:

777170	004040	XXXX	⟨LF⟩
177172	000000	222	⟨CR⟩

*ERR and DONE are asserrted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request will be generated at this point.

CAUTION

The Set Media Density operation takes about 15 seconds and the Format operation takes about 45 seconds. Do not interrupt these functions. If either operation is interrupted, or an error occurs, an illegal diskette is generated and the operation must be repeated.

4.5.6 Read Status (1Ø1)

This function, initiated by leading the command into the RXVCS, updates the drive status information. DONE is negated and RXVES bit 7 (DR RDY) is updated by sampling the drive ready status line. Drive density is updated by loading the head of the selected drive and reading the first data address mark. This operation requires about 250ms to complete.*

4.5.7 Write Deleted Data Sector (11Ø)

This operation is the same as the Write Sector (ØlØ) operation except that the data address mark preceding the data is not the standard data address mark. A single or double density deleted data address mark is written according to the density of the function.

4.5.8 Read Error Code (111)

This function, initiated by loading the RXVCS with the command, retrieves the Extended Status registers. DONE is negated. When TRAN REQ is asserted the program loads the bus address into the RXVDB, which negates TRANS REQ. Under DMA control one word at a time is assembled and transferred to memory starting at the specified address.

If non-existent memory is encounted during the transfer, the operation is aborted, and ERR is asserted.*

When all four words are transferred DONE is set and, if enabled, an Interrupt Request is generated.

*DONE is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request will be generated at this point.