Part Number 2120-0067

DQ419
FLOPPY DISC CONTROLLER
INSTRUCTION MANUAL

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DISTRIBUTED LOGIC CORPORATION
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Contents

Figures

Tables

Section 1 - General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the Model DQ419 floppy disk controller manufactured by Distributed Logic Corp., Anaheim, California. The controller supports one or two dual density, single or double sided floppy disk drives. The single dual-wide module is software and media compatible with the DEC* RXV21/RX02, and features an on-board bootstrap and diskette formatting capability.

The material in this manual is arranged into the following sections:

Section 1 - GENERAL INFORMATION. This section contains a brief description of the controller, its logical track format, recording scheme, and a list of specifications.

Section 2 - INSTALLATION. This section explains the requirements and procedures for equipment installation. Alternate jumper selectable options and cabling are described.

Section 3 - OPERATION. This section explains the controller operation, including bootstrapping and formatting.

Section 4 - PROGRAMMING. A description of the controller control registers and programming features are presented to aid the user in programming the controller.

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1.2 GENERAL DESCRIPTION

The controller is a dual density floppy disk controller compatible with the DEC RX01/RX02. When connected to a Shugart-type drive, it replaces the RXV21 subsystem. The controller provides either single density encoding compatible with IBM 3740 devices, or double density encoding. The controller provides 512K bytes of storage on a single diskette. When two floppy drives are used, each drive may operate at a different density.

The controller is a single dual-wide module that plugs directly into any standard Q bus* slot and interfaces through a 50-conductor ribbon cable to a Shugart compatible drive. The controller is factory preset for the standard device address 177170 and interrupt vector 264. The interrupt level is factory preset to level 4. Alternate addresses and interrupt vectors are jumper selectable. Features include:

Transparent firmware bootstrap that automotically boots double density diskettes (jumper selectable).

Write precompensation to reduce bit shift for greater data integrity.

Power fail protect to inhibit write sequence while the controller completes sector currently being written.

Write current control for tracks greater than 43.

Jumper selectable 4-level interrupt priorities compatible with LSI-11/23 or LSI-11/2.

Supports 22-bit addressing with appropriate software changes.

1.3 COMPATIBILITY

The hardware, software and media compatibility with DEC's RXV21 system is provided to aid the user in data interchange with foreign systems.

HARDWARE. The controller is compatible with the LSI-11, LSI-11/2 and LSI-11/23 CPUs. The single dual-wide module plugs directly into any standard LSI-11 backplane. Alternate address selection and a 4-level device interrupt priority scheme allows expanded system configurations. Shugart 800/850-compatible drive logic is interfaced through a 50-pin ribbon connector.

SOFTWARE. The controller is completely compatible with DEC's RXV21 register definition and command protocol. The SDC-RXV31 will operate, with no modification, with operating systems and diagnostics designed for the RX02.

MEDIA. Media (either preformatted or blank soft sectored diskettes) for the controller is compatible with the IBM 3740. Recommended media are IBM single or double density, or DEC RX01/RX02.

1.4 LOGICAL TRACK FORMAT

Figure 1-1 defines each track format. The sector header field of each sector contains information describing both the sector and track number. All fields are recorded in FM except as noted in the following sections.

1.4.1 Sector Header Field

The header field consists of 7 bytes of information preceded by a field of 6 bytes of "zero" data for synchronization.

Byte 1 ID ADDRESS MARK. A unique mark consisting of 1 byte of FE (hex) data with 3 missing clock transitions using a C7 (hex) clock pattern. This mark is decoded by the controller and indicates the start of the sector header.

Byte 2 TRACK ADDRESS. This byte indicates the absolute (0-114 octal) track address. Each sector contains this track information to locate its position on one of the 77 tracks.

Byte 3 "ZERO"

Byte 4 SECTOR ADDRESS. This byte indicates the absolute (0-32 octal) sector address. Each sector contains this information to identify its position of the track.

Byte 5 "ZERO"

Byte 6,7 CRC. This is the 16-bit cyclic redundancy character and is calculated for each header from the first 5 bytes of information. Calculation, using the IBM 3740 polynomial, is defined in Section 1.4.3.

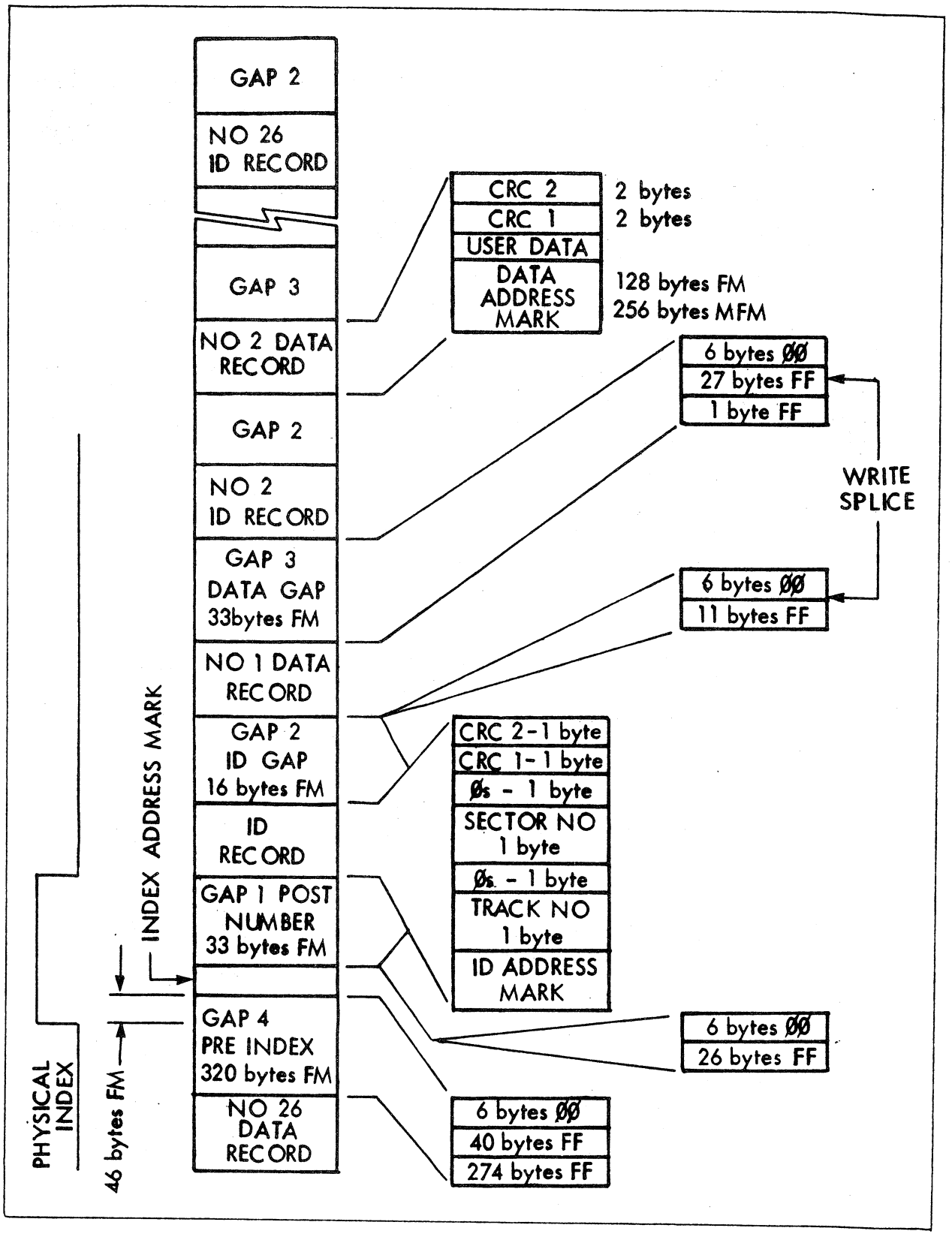


FIGURE 1-1: LOGICAL TRACK FORMAT

1.4.2 Data Field

The data field consists of either 131 or 259 bytes of information (depending on recording method) preceded by 6 bytes of "zero" data for synchronization.

The preamble and data address mark are written in FM. The user data and CRC character are written in either FM or modified MFM, depending on the formatted diskette density.

Byte 1 DATA ADDRESS MARK. This byte is a unique mark consisting of a data byte with three missing clock transitions using a C7 (hex) clock pattern as defined in Table 1-1. This byte is written in FM and is decoded by the controller to indicate the start of the data field, FM vs MFM recording method, and deleted data field indication.

ADDRESS MARK	INDICATED DENSITY	DATA
INDEX	N/A	FC
ID	N/A	FE
DATA	FM	FB
	MFM Modified	FD
DELETED DATA	FM	F8
	MFM Modified	F9

TABLE 1-1: ADDRESS MARKS

Bytes 2-257 FM (BYTES 2-129) OR MODIFIED MFM (BYTES 2-257). This field is recorded in either FM or modified MFM. Either 128 or 256 bytes of information can be stored, depending on the encoding scheme.

Bytes 130-131 or 258-259 CRC. This 16-bit cyclic redundancy character is calculated for each data field from the first 129 or 257 bytes of information using the IBM 3740 polynomial as defined in Section 1.4.3. These bytes are recorded with the same encoding scheme as the data field.

1.4.3 CRC - Cyclic Redundancy Check

Each sector header field and data field has a 2-byte (16-bit) CRC character which is the remainder that results when dividing the data bits (represented as a polynomial M(x)) by a generator polynomial G(x). The polynomial used for IBM 3740 is $G(x) = x^{16} + x^{12} + x^5 + 1$. Data bits include bytes 1-5 for the sector header, bytes 1-129 for an FM data field, and bytes 1-257 for an MFM data field.

1.5 RECORDING SCHEME

Double frequency (FM) and DEC modified Miller code (MFM) recording schemes are used by the controller. FM, used for single density recording, is compatible with IBM 3740 or DEC RX01 media. Modified MFM, used for recording double density, is compatible with the RX02 system.

1.6 SPECIFICATIONS

Power Requirements:	5VDC at 2.5A (from LSI-11 backplane)
Bus Load:	1
Priority Level:	4-level compatible with LSI-11/23 CPU (Selectable alternates)
Interrupt Vector:	264 (Selectable alternate at 270
Device Address:	177170 (Selectable alternate at 177174)
Interface:	Shugart compatible
Media:	RX01/RX02 compatible
Recording Method:	DEC modified MFM (Double density compatible RX02) or optional FM (single density compatible with IBM 3740)
Cable:	Requires standard 50-conductor 3M-type ribbon cable - not supplied.
Temperatures:	0°C to 45°C
Humidity:	10% to 95% noncondensing.

Section 2 - Installation

2.1 CONTROLLER JUMPER CONFIGURATIONS

The controller is shipped configured with DEC standard operating parameters as defined in Table 2-1.

PARAMETER	SELECTION
Control Address	177170
Vector Address	264
Interrupt	Level 4
Firmware Bootstrap	Enabled
Write Precompensation	Enabled
Write Current Control	Enabled

TABLE 2-1: FACTORY SET PARAMETERS

Options are etched to the most often used operation. Etches must be cut before alternate jumpers are inserted. Several of the options are selectable by using AMP 530153-2 pin jumpers or, alternately, No. 30 wire wrap. Refer to Figure 2-1 for jumper locations. Notice that certain jumpers are dedicated for factory test only. Jumpers 11-12, 13-14, and 20-21 must NOT be removed. Jumper 15-16 must NOT be installed.

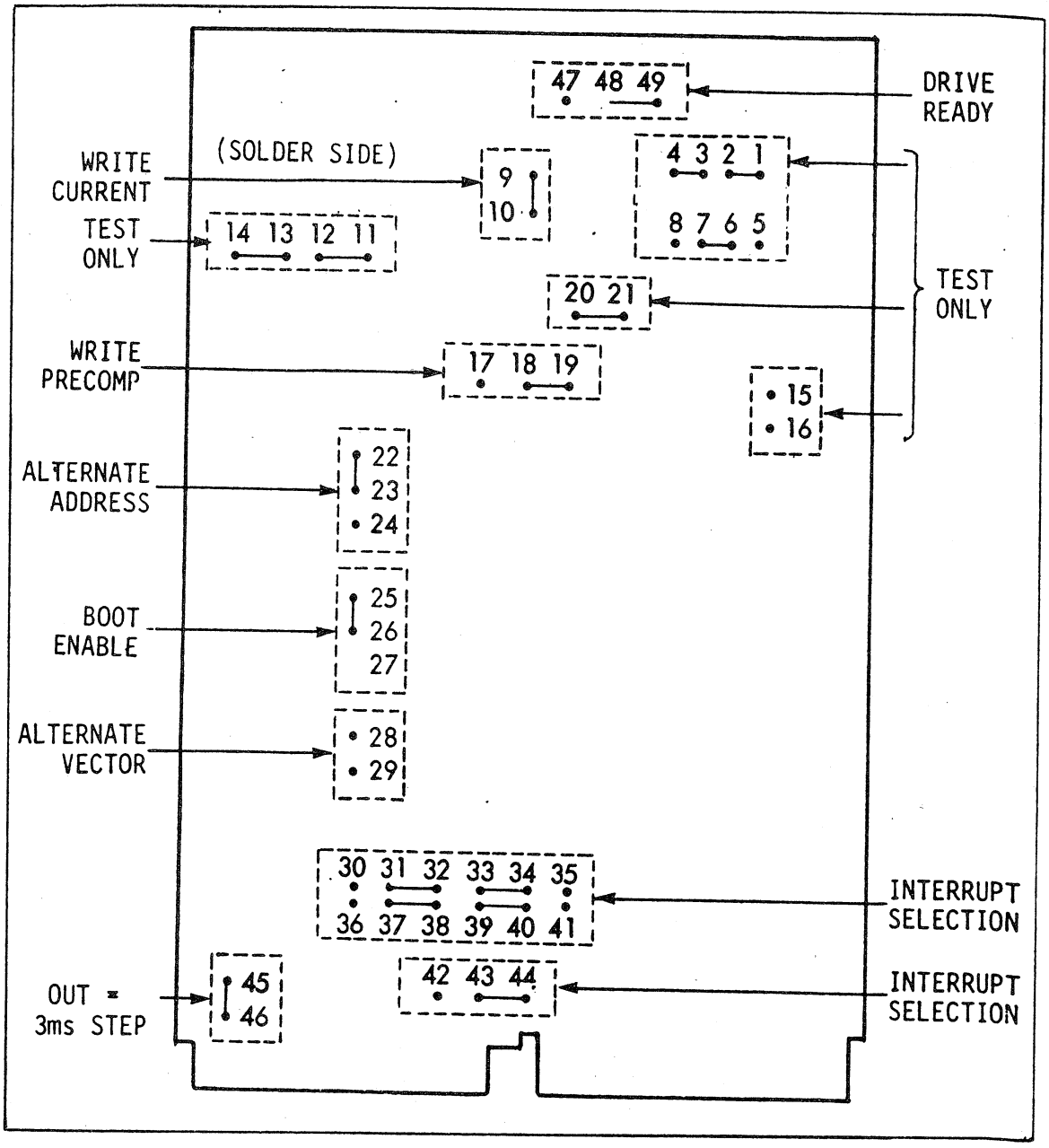


FIGURE 2-1: JUMPER LOCATIONS INDICATING FACTORY SET JUMPERS/ETCHES

2.1.1 Device and Vector Address Selection

The controller is shipped with the DEC standard device and vector addresses preset to 177170 and 264 respectively. Any change in these addresses requires a change in system software. The alternate device and vector addresses are selectable and are defined as 177174 and 270 respectively. These alternate addresses are typically used for systems with more than two drives where two controllers are required. To configure the second controller for address/vector assignments, cut the etch between W22 and W23; then jumper W23-W24 and W28-W29 as shown in Table 2-2.

OPTION	JUMPERS 22-23	23-24	28-29
Standard Device (177170) Vector (264) Addresses*	IN	OUT	OUT
Alternate Device (177174) Vector (270) Address	OUT	IN	IN

*Factory Preset

TABLE 2-2: DEVICE/VECTOR ADDRESS JUMPERS

2.1.2 Device interrupt Priority

The controller supports the 4-level device interrupt priority scheme compatible with the LSI-11/23. The controller asserts interrupt requests and monitors higher level request lines during interrupt arbitration. The level 4 request is always asserted by the controller, regardless of its priority, to maintain compatibility with the LSI-11 and LSI-11/2 CPUs.

The interrupt priority is factory preset to level 4. If an alternate interrupt level is desired, the following etches must be cut: W31-W32, W33-W34, W37-W38, W39-W40, and W43-W44. Refer to Table 2-3 for the jumper installation for the desired priority level.

PRIORITY LEVEL	ASSERT LEVEL	MONITOR LEVEL	JUMPERS W30 W31	W31 W32	W33 W34	W34 W35	W36 W37	W37 W38	W39 W40	W40 W41	W42 W43	W43 W44
4*	4	5,6	OUT	IN	IN	OUT	OUT	IN	IN	OUT	OUT	IN
5	4,5	6	OUT	IN	IN	OUT	IN	OUT	OUT	IN	OUT	IN
6	4,6	7	IN	OUT	OUT	IN	OUT	IN	IN	OUT	IN	OUT
7	4,6,7	NONE	IN	OUT	OUT	IN	IN	OUT	OUT	IN	IN	OUT

*Factory Preset

TABLE 2-3: PRIORITY LEVEL CONFIGURATIONS

2.1.3 Bootstrap

The controller module contains a transparent firmware bootstrap which is initiated whenever program execution is started at location 173000, homing both drives to track 0. Track 1, sector 1 of unit 0 is then read and diskette density is determined. For single density diskettes sectors 1, 3, 5 and 7 are loaded into memory starting at location 0. If the diskette is double density, sectors 1 and 3 are loaded. Program execution is then transferred to location 0.

BOOTSTRAP	-------JUMPERS-------	
	W25-W26	W26-W27
Enable*	IN	OUT
Disable	OUT	IN

*Factory Jumpered

TABLE 2-4: BOOTSTRAP CONFIGURATIONS

NOTE

Only one bootstrap should be enabled in a system for proper operation. If a second bootstrap exists in the system, it must be disabled before enabling the controller bootstrap.

2.1.4 Write Precompensation

The controller provides hardware write precompensation to reduce bit shift. The controller is shipped with write precompensation enabled. It is recommended that, for reliable operation, this feature not be disabled. However, if write precompensation must be disabled, remove the etch W18-W19 and insert jumper W17-W18 as shown in Table 2-5.

WRITE PRECOMPENSATION	-------JUMPERS-------	
	W17-W18	W18-W19
Enable*	OUT	IN
Disable	IN	OUT

*Factor Jumpered

TABLE 2-5: WRITE PRECOMPENSATION CONFIGURATION

2.1.5 Write Current Control

The controller provides the necessary signal to reduce the write current for tracks greater than 43. This signal is available at pin 2 of the 50-pin connector. Write current jumper configurations are shown in Table 2-6

WRITE CURRENT	JUMPER W9-W10
Enable*	IN
Disable	OUT

*Factory preset

TABLE 2-6: WRITE CURRENT CONFIGURATIONS

2.1.6 Drive Step Rate

The floppy disk controller is designed to automatically select step rate of 3ms or 6ms. An assumption is made that all double-sided floppy disk drives step at 3ms, and all single-sided drives step at 6ms. If a 3ms step is required for a single-sided drive, remove jumper W45-W46 as shown in Table 2-7.

STEP RATE SELECT	W45-W46
Single-side 3ms	OUT
All others	IN

TABLE 2-7: 3ms STEP CONFIGURATION

2.2 DRIVE CONFIGURATIONS

For proper operation the floppy drive(s) must be configured correctly. The controller uses radial drive selection and the drive(s) must be set up with this in mind. When two drives are used, the first drive is denoted 0 and the second drive 1. A particular drive is selected and remains selected after a function is complete, thus allowing the controller to poll drive status. A separate head load signal is provided by the controller read and write functions on the diskette. The "in use" logic of the drive is configured as a function of head loading. Since the drives are homed without loading the heads during an initialize command, the drive is configured to provide stepper motor power independent of head loading. Strapping configurations are shown in the following tables for some of the most comman configurations.

SHUGART JUMPER	DESCRIPTION	DUAL DRIVES DR 0	DUAL DRIVES DR 1	SINGLE DR 0
DS1	Drive Select 1	IN	OUT	IN
DS2	Drive Select 2	OUT	IN	OUT
DS3	Drive Select 3	OUT	OUT	OUT
DS4	Drive Select 4	OUT	OUT	OUT
A	Radial Head Loading Option	IN	IN	IN
B	Radial Head Loading Option	IN	IN	IN
C	Head Load Option	IN	IN	IN
D	In Use Option	OUT	OUT	OUT
X	Radial Head Loading Option	OUT	OUT	OUT
WP	Inhibit Write When Protected	IN	IN	IN
NP	Allow Write When Protected	OUT	OUT	OUT
DS	Stepper Power from Drive Select	IN	IN	IN
HL	Stepper Power from Head Load	OUT	OUT	OUT
Z	In Use from Drive Select	OUT	OUT	OUT
Y	In Use from Head Load	IN	IN	IN
R	Ready Output	IN	IN	IN
I	Index Output	IN	IN	IN
DC	Disk Change Output	X	X	X
S	Sector Output	X	X	X
800	Sector Option Disable	IN	IN	IN
801	Sector Option Enable	OUT	OUT	OUT
L	-5V DC Bias	IN	IN	IN
51	Termination HL	OUT	IN	IN
52	Termination Drive Select	IN	IN	IN
T3	Termination Direction	OUT	IN	IN
T4	Termination Step	OUT	IN	IN
T5	Termination Write Data	OUT	IN	IN
T6	Termination Write Gate	OUT	IN	IN

TABLE 2-8: CONFIGURATIONS FOR SHUGART SA800/801 DRIVES

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR 0	DR 1	SINGLE DR 0
SE	Termination for MUXed standard input	IN	OUT	IN
DS1	Drive select 1 input pin	IN	OUT	IN
DS2	Drive select 2 input pin	OUT	IN	N/A
1B,2B 3B,4B	Side select option-drive select	OUT	OUT	OUT
RR	Radial ready	IN	IN	IN
R1	Radial index and sector	IN	IN	IN
R*	Option shunt for ready output	IN	IN	IN
2S	Two-sided status output	IN	IN	IN
850/51	Sector option enable	IN	IN	IN
I*	Index output	IN	IN	IN
S*	Sector output	OUT	OUT	OUT
DC	Disk change option	OUT	OUT	OUT
HL*	Stepper power from head load	OUT	OUT	OUT
DS	Stepper power from drive select	IN	IN	IN
WP	Inhibit write when write protected	IN	IN	IN
NP	Allow write when write protected	OUT	OUT	OUT
D	Alternate input - in use	OUT	OUT	OUT
M	Multi-media option	IN	IN	IN
DL	Door lock latch option	OUT	OUT	OUT
A,B*	Radial head load	IN	IN	IN
X*	Radial head load	OUT	OUT	OUT
C	Alternate input - head load	IN	IN	IN
Z*	In use from drive select	OUT	OUT	OUT
Y	In use from head load	IN	IN	IN
S1	Side select option using direction select	OUT	OUT	OUT
S2	Standard side select input	IN	IN	IN
S3	Side select option using drive select	OUT	OUT	OUT
TS,FS	Data separation option select	OUT	OUT	OUT
IW	Write current switch	IN	IN	IN
RS	Ready standard	IN	IN	IN
RM	Ready modified	OUT	OUT	OUT
HLL	Head load latch	OUT	OUT	OUT
IT	In use terminator	OUT	OUT	OUT
HI	Head load or in use to in use circuit	OUT	OUT	OUT
F	Remove for MFM encoding	OUT	OUT	OUT
AF	Install for FM or MFM encoding	IN	IN	IN
NF	Install for M2FM encoding	OUT	OUT	OUT

*Shunt

TABLE 2-9: CONFIGURATION FOR SHUGART SA850/851 DRIVES

NOTE

For SA850/851 drives a 16-pin programmable shunt, location 4F, is provided for the eight most commonly used cut track options. These traces are usually shorted as shipped from the factory. The traces can be opened as follows:

Jumper Z-Open Pin 1 to Pin 16
Jumper A-Open Pin 3 to Pin 14
Jumper X-Open Pin 5 to Pin 12
Jumper R-Open Pin 7 to Pin 10
Jumper HL-Open Pin 2 to Pin 15
Jumper B-Open Pin 4 to Pin 13
Jumper I-Open Pin 6 to Pin 11
Jumper S-Open Pin 8 to Pin 9

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR 0	DUAL DRIVES DR 1	SINGLE DR 0
U9	Terminations for multiplexed inputs	OUT	IN	IN
SI	Internal write current switch	IN	IN	IN
SE	External write current switch	OUT	OUT	OUT
TR	True ready output	IN	IN	IN
2S	Two-sided status output	IN	IN	IN
DC	Disk change option	OUT	OUT	OUT
S1	Side select option using direction select	OUT	OUT	OUT
S2	Side select input	IN	IN	IN
S3	Side selection option using drive select	OUT	OUT	OUT
1B,2B 3B,4B	Side selection option using drive select	OUT	OUT	OUT
D	Alternate input in use	OUT	OUT	OUT
MS	Motor on from drive select	IN	IN	IN
MO	Alternate input-motor on	OUT	OUT	OUT
MD	Motor off delay	OUT	OUT	OUT
R	Ready output	IN	IN	IN
Y	In use from head load	IN	IN	IN
RR	Radial ready	IN	IN	IN
DS1	Drive select 1 input	IN	OUT	IN
DS2,3 DS4	Drive select 2,3,4 input	OUT	DS2	OUT
PD	Stepper power down	OUT	OUT	OUT
WP	Inhibit write when write protected	IN	IN	IN
NP	Allow write when write protected	OUT	OUT	OUT
TS	Data separation option select	OUT	OUT	OUT

TABLE 2-10: CONFIGURATION FOR SHUGART 810/860 FLOPPY DRIVES

QUME JUMPER	DESCRIPTION	DUAL DRIVES DR 0	DUAL DRIVES DR 1	SINGLE DR 0
DS1	Drive Select 1	IN	OUT	IN
DS2	Drive Select 2	OUT	IN	OUT
DS3	Drive Select 3	OUT	OUT	OUT
DS4	Drive Select 4	OUT	OUT	OUT
A	Radial Head Load option	IN	IN	IN
B	Radial Head Load Option	IN	IN	IN
X	Radial Head Load Option	OUT	OUT	OUT
Z	In Use from Drive Select	OUT	OUT	OUT
HL	Stepper Power from Head Load	OUT	OUT	OUT
R	Ready Alternate Output Pad	IN	IN	IN
I	Index Alternate Output Pad	IN	IN	IN
C	Alternate Input Head Load	IN	IN	IN
C	Alternate Input in Use	OUT	OUT	OUT
DC	Alternate Output Disk Change	IN	IN	IN
2S	Alternate Output 2-Sided Disk Status	IN	IN	IN
DS	Stepper Power from Drive Select	IN	IN	IN
Y	In Use from Head Load	IN	IN	IN
DL	Door Lock Latch	OUT	OUT	OUT
RR	Radial Ready	IN	IN	IN
RR	Radial Index	IN	IN	IN
HP	Inhibit Write when Write Protected	IN	IN	IN
NP	Allow Write when Write Protected	OUT	OUT	OUT
D1,D2 D4,DDS	Drive Address, Select Pads (up to 8 Drives)	OUT	OUT	OUT
B1,B2 B3,B4	Two Headed Drive Select	OUT	OUT	OUT
S1	Head Select Option	OUT	OUT	OUT
S2	Head Select Option	IN	IN	IN
S3	Head Select Option	OUT	OUT	OUT
1TM	Termination Resistor Pack	OUT	IN*	IN
2TM	Termination Resistor Pack	OUT	IN*	IN

*Termination resistor pack must be installed on drive 1 and removed from drive 0 on dual floppy systems. On single floppy systems, install the termination resistor on drive 0.

TABLE 2-11: CONFIGURATIONS FOR QUME (DATA TRAK 8) AND VE-DATA (YD-174) INTERFACE DRIVES

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR 0	DR 1	SINGLE DR 0
DS1-DS4	Drive select address pins (up to 4 drives)	DS1	DS2	DS1
A,B	Radial head load	IN	IN	IN
X	Radial head load	OUT	OUT	OUT
Z	In use from drive select	OUT	OUT	OUT
HL	Stepper power from head load	OUT	OUT	OUT
R	Alternate output ready pad	IN	IN	IN
I	Alternate output index pad	IN	IN	IN
C	Alternate input head load	IN	IN	IN
D	Alternate input in use	OUT	OUT	OUT
DC	Alternate output disk change	OUT	OUT	OUT
2S	Alternate output two sided disk	IN	IN	IN
Y	In use from head load	IN	IN	IN
DL	Door lock latch	OUT	OUT	OUT
RR	Radial ready	IN	IN	IN
RI	Radial index	IN	IN	IN
WP	Inhibit write when write protect	IN	IN	IN
NP	Allow write when write protect	OUT	OUT	OUT
D1,D2	Drive address select			
D4,DDS	(up to 8 drives)	OUT	OUT	OUT
B1-B4	Two, double-sided drive select	OUT	OUT	OUT
S1,S3	Head select option	OUT	OUT	OUT
S2	Head select option	IN	IN	IN
T40	Test track 40	OUT	OUT	OUT
HA	Test actuate head load	OUT	OUT	OUT
4,6,8,10 12,16 18,24	Alternate I/O pins	OUT	OUT	OUT
SF	Switch filter	IN	IN	IN
SP	Stepper power (used with HL)	OUT	OUT	OUT

TABLE 2-12: CONFIGURATION FOR QUME TRAK 242 FLOPPY DRIVES

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR 0	DR 1	SINGLE DR 0
TM	Termination for muxed standard input	OUT	IN	IN
DS1	Drive select 1 input pin	IN	OUT	IN
DS2	Drive select 2 input pin	OUT	IN	N/A
1B,2B 3B,4B	Side select option-drive select	OUT	OUT	OUT
RR	Radial ready	IN	IN	IN
R1	Radial index and sector	IN	IN	IN
R	Option shunt for ready output	IN	IN	IN
2S	Two-sided status output	IN	IN	IN
DC	Disk change option	OUT	OUT	OUT
HL	Stepper power from head load	OUT	OUT	OUT
WP	Inhibit write when write protected	IN	IN	IN
NP	Allow write when write protected	OUT	OUT	OUT
D	Alternate input - in use	OUT	OUT	OUT
DL	Door lock latch option	OUT	OUT	OUT
A,B	Radial head load	IN	IN	IN
X	Radial head load	OUT	OUT	OUT
C	Alternate input - head load	IN	IN	IN
Z	In use from drive select	OUT	OUT	OUT
Y*	In use from head load	IN	IN	IN
S1	Side select option using direction select	OUT	OUT	OUT
S2	Standard side select input	IN	IN	IN
S3	Side select option using drive select	OUT	OUT	OUT
RS	Ready standard	IN	IN	IN
RM	Ready modified	OUT	OUT	OUT
HLL	Head load latch	OUT	OUT	OUT
HI	Head load or in use to in use circuit	OUT	OUT	OUT
IT	In use terminal	IN	IN	IN
I	Index output	IN	IN	IN
RFa	"Don't remove"	IN	IN	IN
RFb	"Keep open"	OUT	OUT	OUT
MD	Motor on from head load	OUT	OUT	OUT
MS	Motor on from drive select	OUT	OUT	OUT
BS0	"Don't cut"	IN	IN	IN
BS1	"Keep open"	OUT	OUT	OUT
V	Door lock from head load	IN	IN	IN

*Solder jumper in

TABLE 2-13: CONFIGURATIONS FOR MITSUBISHI HALF HEIGHT M2896-63 FLOPPY DRIVE

TRACE DESIG	DESCRIPTION	DUAL DRIVES DR 0	DUAL DRIVES DR 1	SINGLE DR 0
TM	Termination for muxed standard input	OUT	IN	IN
DS1	Drive select 1 input pin	IN	OUT	IN
DS2	Drive select 2 input pin	OUT	IN	N/A
1B,2B 3B,4B	Side select option - drive select	OUT	OUT	OUT
RR	Radial ready	IN	IN	IN
RI	Radial index and sector	IN	IN	IN
R*	Option shunt for ready output	IN	IN	IN
2S	Two-sided status output	IN	IN	IN
I*	Index output	IN	IN	IN
DC	Disk change option	IN	IN	IN
HL*	Stepper power from head load	IN	IN	IN
DS	Stepper power from drive select	OUT	OUT	OUT
WP	Inhibit write when write protected	IN	IN	IN
NP	Allow write when write protected	OUT	OUT	OUT
D	Alternate input - in use	OUT	OUT	OUT
DL	Door lock latch option	OUT	OUT	OUT
A,B*	Radial head load	IN	IN	IN
X*	Radial head load	IN	IN	IN
C	Alternate input - head load	OUT	OUT	OUT
Z*	In use from drive select	IN	IN	IN
Y	In use from head load	OUT	OUT	OUT
S1	Side select option using direction select	OUT	OUT	OUT
S2	Standard side select input	IN	IN	IN
S3	Side select option using drive select	OUT	OUT	OUT
RM	Ready modified	OUT	OUT	OUT
M1	Spindle motor control option	IN	IN	IN
M2	Spindle motor control option	OUT	OUT	OUT
M3	Spindle motor control option	IN	IN	IN
M4	Spindle motor control option	OUT	OUT	OUT
MC1-4	Motor control select	OUT	OUT	OUT

*Denotes shunt

TABLE 2-14: CONFIGURATION FOR TANDON HALF HEIGHT 848 FLOPPY DISK DRIVE

2.3 CABLING

An optional 50-conductor ribbon cable connects the controller to a Shugart compatible drive. Connect the cable to the 50-pin connector located at the top of the controller board observing the alignment of pin 1 as indicated in Figure 2-2. The cable can be purchased from an independent source, or the following list of materials (or equivalent) will aid in the construction of the required cable.

QTY	DESCRIPTION	MFG	P/N
1	50-pin controller connector	3M	3425-3000
2	50-pin drive connectors	3M	3415-001
A/R	50-conductor ribbon cable	3M	3365/50

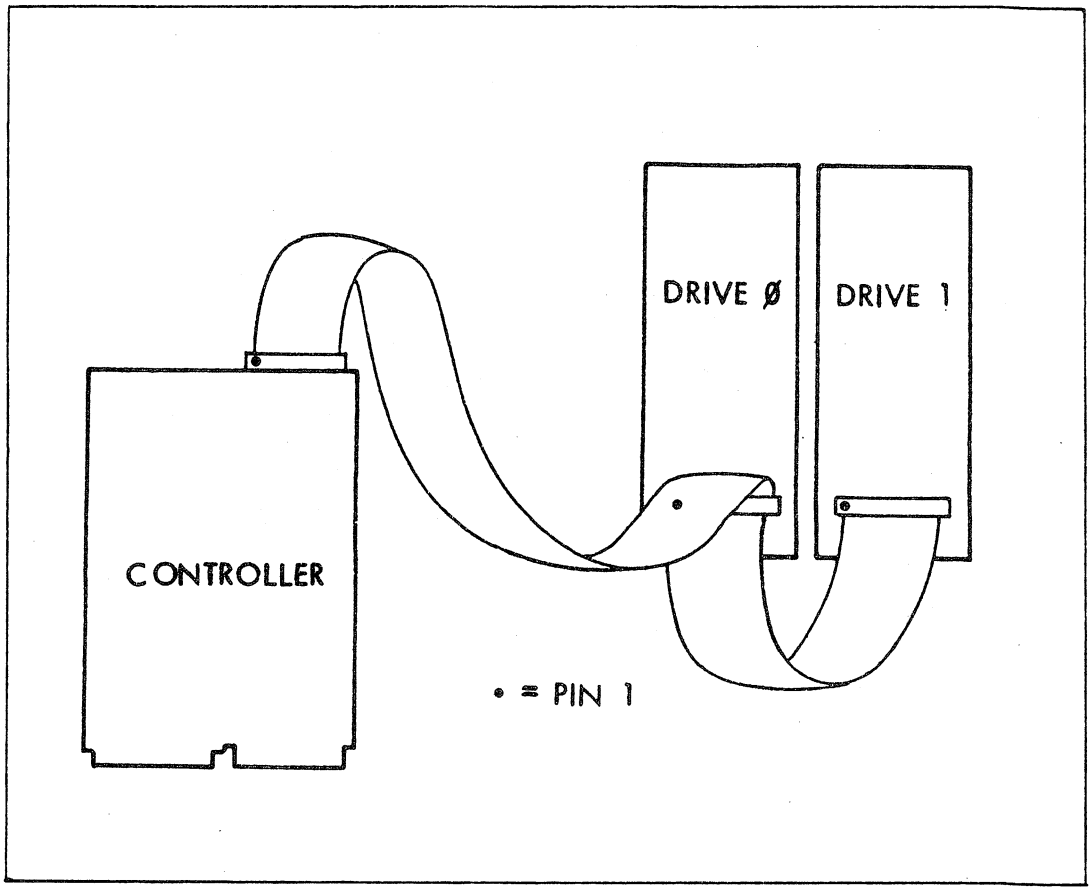


FIGURE 2-2: DRIVE/CONTROLLER CABLING

The connector pins illustrated in Figure 2-3 are compatible with Shugart-type 800/850 series interfaces.

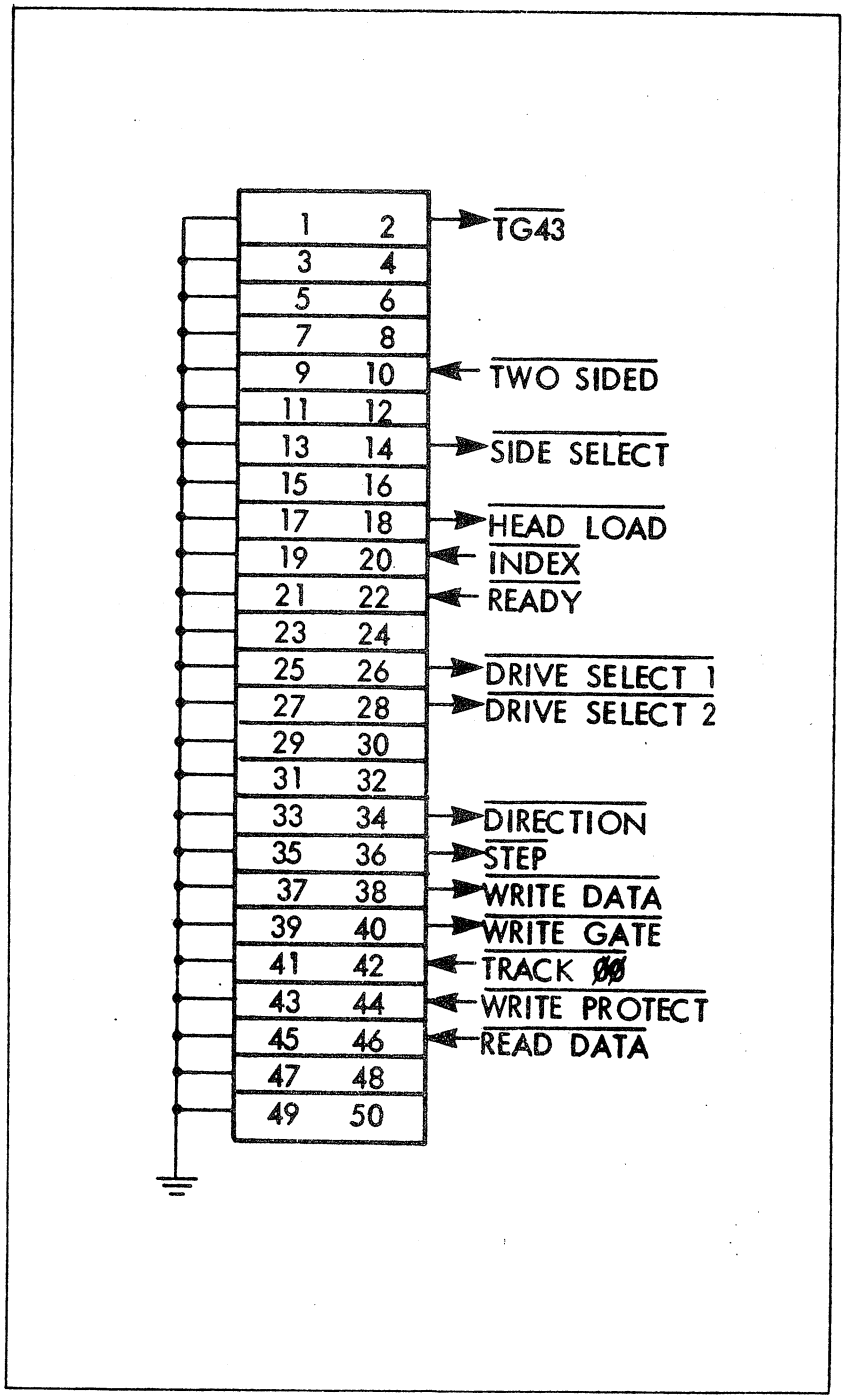


FIGURE 2-3: CONNECTOR PIN DEFINITIONS

2.4 CONTROLLER INSTALLATION

The controller can be installed directly into any Q bus slot provided that interrupt and DMA continuity is maintained. These signals are daisy chained through the LSI-11 backplane and there should be no unused slots between the processor and the floppy controller. Priority sequences for the backplane can be found in the documentation accompanying the LSI-11 system. Note that when two interrupts of the same priority level are asserted, the device closer to the CPU receives the higher priority.

2.5 INITIAL CHECKOUT

After the controller jumpers and drive selection have been configured, initial checkout is performed using the following procedure.

NOTE

The bootstrap must be disabled for the following procedure.

1. Apply AC and DC power to the drive(s). The spindle should begin to rotate. The "in use" indicators on both drivesshould be off.

2. Place the RUN/HALT switch on the CPU to the HALT position, and turn on the processor. An character on the terminal signifies that console ODT has been entered. First drive 1, then drive 0, will step the heads inward 10 tracks; then step the heads outward until the home signal is detected. If heads will not load and/or "in-use" indicators do not light, check cabling and drive power supplies.

3. Place a preformatted scratch diskette in drive 0.

4. If the standard address assignment is selected, open the Control Status (CS) register using ODT by typing 177170. The terminal will display 004040 (the contents of the CS register). Deposit a 40000 in the CS by typing 40000<CR>. This command will initialize the controller. First drive 1, then drive 0 will calibrate for home position by stepping inward 10 tracks and then outward one track at a time until the drive indicates track 0 has been reached. After calibration the head on drive 0 is loaded. Sector 1 of track 1 is read into the controller buffer, as indicated by the in-use LED on drive 0. The LED will remain on for a short time after the read operation is complete.

   If, after initializing, the drives do not calibrate or the LED does not light, check the cabling and power supplies.

5. Reopen the CS (177170) using ODT as described above. The contents of this location should be 004040. Examine the next location (177172) by using the linefeed key or by typing 177172</>, which should yield either 204 or 244. For a detailed description of register protocol and bit definition, refer to Section 4.

6. Either diagnostics or an operating system can now be booted.

Section 3 - Operation

3.1 GENERAL INFORMATION

This section provides the operating instructions for the controller. Included are bootstrapping, formatting, fill/write, and read/empty operations. This section also reviews operation with an RT-11 operating system.

3.2 BOOTSTRAPPING

If the bootstrap is enabled, the controller will respond to the standard bootstrap address 173000. The controller is booted by typing 173000G while in console ODT, causing a bus INIT and program execution transfer to 173000. An alternate method is to strap the LSI-11 CPU to power up in Mode 2, whereupon power-up the CPU automatically starts execution at 173000. Power-up strapping procedures for the LSI-11 processor can be found in the "Microcomputer Processor Handbook."*

To boot either a single or double density diskette, use the following procedure:

1. Place the diskette in drive 0.
2. If the processor is strapped for power-up Mode 2, operate the INIT (boot) switch or cycle DC power OFF and ON.
3. If the processor is not strapped for power-up Mode 2 while in console ODT, type 173000G.

*Published by Digital Equipment Corporation, Maynard, MA.

3.3 FORMATTING

The controller is capable of formatting diskettes in a specified density. The formatting is accomplished on two passes. During pass 1, an index address mark is written on track 0 following the index hole. Twenty-six sector headers are written following the index address. Each of the remaining 76 tracks is written in the same manner. When track 76 is completed, pass 2 is initiated. The controller seeks track 0 and writes zero data field in sector 1 using the selected density. The remaining sectors are written in the same manner.

The format command selects diskette density, unit and side (for dual drives). Table 3-1 defines the command words.

DENSITY/SIDE	UNIT 0	UNIT 1
Single Density Side 0	11	31
Single Density Side 1	1011	1031
Double Density Side 0	411	431
Double Density Side 1	1411	1431

TABLE 3-1: DENSITY/SIDE COMMANDS

Figure 3-1 illustrates a format subroutine. The format command is loaded into TXVCS. When TRAN REQ is set, the keyword 222 is loaded into RXVDB. When the diskette is formatted, a return is made.

```
FORMAT:

        MOV     #11, CMD                ;FORMAT
        BIS     DENS, CMD               ;DENSITY
        BIS     UNIT, CMD               ;UNIT
        BIS     SIDE, CMD               ;SIDE
        MOV     CMD, @#RXVCS            ;SELECT FUNCTION
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     #222, @#RXVDB           ;KEYWORD
        JSR     PC, DNWAIT              ;WAIT FOR DONE
        TST     @#RXVCS                 ;ERROR
        BMI     FRMERR                  ;BR IF SO
        RTS     PC

FRMERR:
```

FIGURE 3-1: FORMAT SUBROUTINE

Alternately, a diskette can be formatted using console ODT. Open the Control and Status (CS) register and deposit the appropriate command. Then deposit the format key word, 222, in the Data Buffer (DB) register. The following is an example of formatting unit 0 side 0 in double density:

```
177170      004040      411<LF>
177172      000000      222<CR>
```

3.4 FILL/WRITE OPERATION

Figure 3-2 illustrates subroutines to write data on a diskette by performing a Fill Buffer followed by a Write Sector operation.

```
FILLBF:

        MOV     #1, CMD                 ;FILL BUFFER
        BIS     DENS, CMD               ;DENSITY
        MOV     CMD,  #RXVCS            ;SELECT FUNCTION
        JSR     PC TRWAIT               ;WAIT FOR TR
        MOV     COUNT,  #RXVDB          ;WORD COUNT
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     #BUFOUT,  #RXVDB        ;BUS ADDRESS OF DATA
        JSR     PC,DNWAIT               ;WAIT FOR DONE
        TST      #RXVCS                 ;ERROR
        BMI     ERFIL                   ;BR IF SO
        RTS     PC

ERFIL:

WSECT:

        MOV     #5, CMD                 ;WRITE, SECTOR
        BIS     DENS, CMD               ;DENSITY
        BIS     UNIT, CMD               ;UNIT
        BIS     SIDE, CMD               ;SIDE
        MOV     CMD, @#RXVCS            ;SELECT FUNCTION
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     SECTOR,  #RXVDB         ;SECTOR
        JSR     PC TRWAIT               ;WAIT FOR TR
        MOV     TRACK @#RXVDB           ;TRACK
        JSR     PC, DNWAIT              ;WAIT FOR DONE
        TST     @#RXVCS                 ;ERROR
        BMI     WSERR                   ;BR IF SO
        RTS     PC

WSERR:
```

FIGURE 3-2: WRITE DATA SUBROUTINES

3.5 READ/EMPTY OPERATIONS

Figure 3-3 describes subroutines to read data from a diskette. This is done by performing a Read Sector operation, followed by an Empty Buffer operation.

```
RSECT:

        MOV     #7, CMD                 ;READ SECTOR
        BIS     DENS, CMD               ;DENSITY
        BIS     UNIT, CMD               ;UNIT
        BIS     SIDE, CMD               ;SIDE
        MOV     CMD, #RXVCS             ;SELECT FUNCTION
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     SECTOR, #RXVDB          ;SECTOR
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     TRACK, #RXVDB           ;TRACK
        JSR     PC, DNWAIT              ;WAIT FOR DONE
        TST       #RXVCS                ;ERROR
        BMI     RSERR                   ;BR IF SO
        RTS     PC

RSERR:

EMPBF:

        MOV     #3, CMD                 ;EMPTY BUFFER
        BIS     DENS, CMD               ;DENSITY
        MOV     CMD, @#RXVCS            ;SELECT FUNCTION
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     COUNT,@#RXVDB           ;WORD COUNT
        JSR     PC, TRWAIT              ;WAIT FOR TR
        MOV     #BUFFIN,@#RXVDB         ;BUS ADDRESS FOR DATA
        TST     @#RXVCS                 ;ERROR
        BMI     EREMP                   ;BR IS SO
        RST     PC

EREMP:
```

FIGURE 3-3: READ DATA SUBROUTINES

3.6 OPERATION USING RT-11

The controller requires a different handler than the single density controllers. This handler is configured to use the DMA transfer scheme of the controller. Also, diskette density is determined by the handler without system intervention, allowing the use of either single or double density diskettes interchangeably.

This handler (designated "DY") is available in RT11-V.3B and later revisions. Use the following procedure to create a DY-based system.

Using an RX01 (or equivalent) system, or a sysem which has an RX01 (or equivalent) peripheral device, copy the monitor file and other associated system files onto a single density diskette. These files can be obtained from the binary distribution media or by performing a SYSGEN and specifying DY as the system device. The following commands will initialize the diskette and copy the necessary files to Drive 1:

```
.INIT/NOQUERY DX1:
.COPY/SYS SYS: SWAP.SYS DX1:
.COPY/SYS SYS: DYMNXX.SYS DX1:
.COPY/SYS SYS: TT.SYS DX1:
.COPY/SYS: DIR.SAV DX1:
.COPY SYS: PIP.SAV DX1:
.COPY SYS: DUP.SAV DX1:
```

The bootstrap must then be copied from the monitor file to block 0 of the diskette. The following command will accomplish this on the diskette in drive 1.

```
.COPY/BOOT DX1: DYMNXX DX1:
```

This diskette can be used with the controller, but it is single density. To build a double density diskette, first format a diskette to double density as explained in Section 3.3. Boot the single density system diskette in drive 0. Use the following commands to initialize the formatted diskette in drive 1 and copy the system software from drive 0 to drive 1.

```
.INIT/NOQUERY DY1:
.COPY/SYS DY:*.*DY1:
```

Finally, copy the bootstrap to block 0 of the diskette in drive 1.

```
.COPY/BOOT DY1: DYMNXX DY1:
```

The diskette in drive 1 can now be booted as a double density diskette.

4.1 GENERAL INFORMATION

This section defines device registers and command protocol for the controller.

Software control of the controller is performed by means of two device registers: the Command and Status (RXVCS) register and a multipurpose Data Buffer (RXVDB) register with addresses 177170 and 177172, respectively. With few exceptions, the registers can be read or write using instructions referring to their addresses.

The RXVCS passes control information from the CPU to the controller and reports status and error information from the controller to the CPU. The RXVDB provides additional control and status information between the CPU and the controller. Information in the RXVDB is a function of the controller operation in progress.

The controller contains a sector buffer capable of storing a complete sector. For Read/Write operations the buffer is either filled before a Write command or emptied after a Read command under DMA control. During a Read, the desired sector is located, and the sector data are transferred to the buffer.

A detailed description of bit assignments are given for registers:

Command and Status	RXVCS	177170
Data Buffer	RXVDB	
Track Address	RXVTA	
Sector Address	RXVSA	
Word Count	RXVWC	177172
Bus Address	RXVBA	
Error and Status	RXVES	
Bus Address Extension	RXVBAE	

4.2 COMMAND AND STATUS REGISTER - RXVCS (177170)

Functions are initiated by loading the Command and Status register, when not busy (bit 5 = 1), with bit 0 = 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	INIT	EXT	ADD	RX02	22BIT	HDSEL	DENSEL	TRREQ	INTENB	DN	UNSEL	FNCT SEL			GO

ERR — ERROR. This bit is set by the controller if an error occurs during an attempt to execute a commands. Cleared by INIT or the initiation of a new command. When an error is detected the RXVCS is read into the RXVDB. Read only.

INIT — INITIALIZE. This bit, set by the program, initializes the controller without initializing all the devices on the LSI-11 bus. Write Only.

CAUTION

Loading the lower byte of the RXVCS will also load the upper byte of the RXVCS.

When set, the controller will negate DONE and move the head position mechanism of drive 1 (if two drives are available) to track 0. When completed, the controller will repeat the operation on drive 0. The controller then clears the Error and Status register, sets Initialize Done and Drive Ready, if drive 0 is ready. Finally the controller reads sector 1, track 1 of drive 0.

EXT ADD — EXTENDED ADDRESS. These bits define an extended bus address; bit 12 = MA16, bit 13 = MA17. Write Only.

RX02 — RX02. This bit, asserted by the controller, indicates an RX02-type system. Read Only.

22-BIT — 22-BIT ADDRESSING. Written as 1 for 22-bit addressing, and written as 0 for 18-bit addressing. See section 4.5.9.

HD SEL — HEAD SELECT. This bit determines the side of the disk for execution of the desired function; bit cleared = side 0, bit set = side 1. Read/Write

DEN SEL — DENSITY SELECT. This bit defines either single or density density operation. Bit cleared = single density, bit set = double density. Read/Write.

TR REQ — TRANSFER REQUEST. This bit indicates the controller needs data or has data available. Read Only.

INT ENB — INTERRUPT ENABLE. This bit, set by the program, enables an interrupt when the controller completes an operation and asserts DONE. Cleared by INIT. Read/Write.

DONE — DONE. This bit indicates the completion of a function. It generates an interrupt when asserted if INT ENB is set. Read Only.

UN SEL — UNIT SELECT. This bit selects one of two disks for execution of the desired function. Read/Write.

FNCT SEL — FUNCTION SELECT. These bits define one of eight operations listed below and described in detail in Section 4.3.

000 = Fill Buffer
001 = Empty Buffer
010 = Write Sector
011 = Read Sector
100 = Set Media Density/Format
101 = Read Status
110 = Write Deleted Data Sector
111 = Read Error Code

GO — GO. Initiates a command to the controller. Write Only.

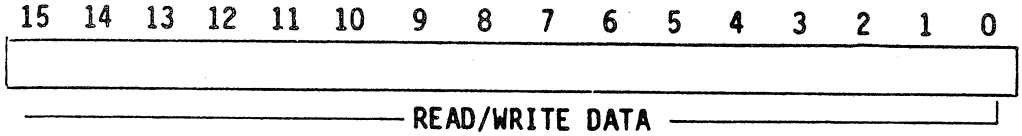
4.3 DATA BUFFER (177172)

This register is a general purpose data path between the controller and the LSI-11. It represents one of six registers (RXVDB, RXVTA, RXVSA, RXVWC, RXVBA, and RXVES). These registers are addressable only under the protocol of the function in progress.

This register is Read/Write if the controller is not in the process of executing a command (i.e., it may be manipulated without affecting the controller). When the controller is executing a command, this register is Read/Write only if RXVCS, bit 7 (Transfer Request), is set.

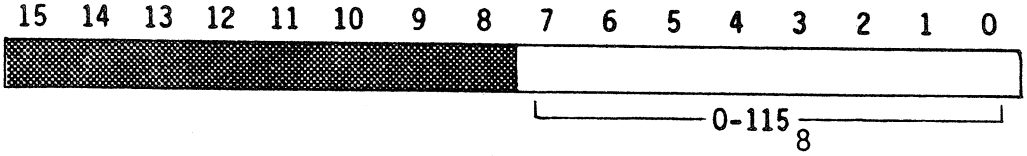
4.3.1 Data Buffer Register (RXVDB)

All information transferred to and from the floppy media passes through the RXVDB register.



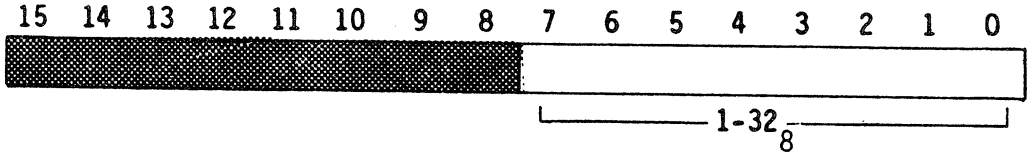
4.3.2 Track Address Register (RXVTA)

This register is loaded to indicate on which of the 115_8 (octal) - 77_{10} decimal - tracks a given function operates.



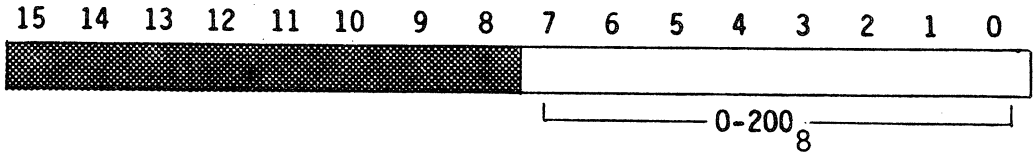
4.3.3 Sector Address Register (RXVSA)

This register is loaded to indicate on which of the 32_8 (octal) - 26_{10} decimal - sectors a given function operates.



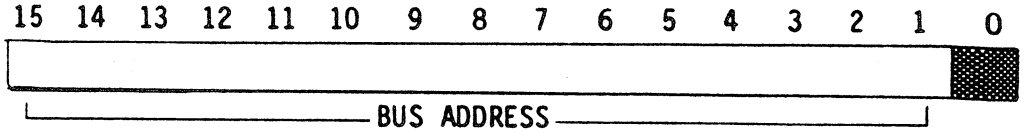
4.3.4 Word Count Register (RXVWC)

This 8-bit register is loaded with the number of words (128_{10} maximum) to be transferred. At the end of each transfer the Word Count register is decremented. When the contents of RXVWC are decremented to zero, transfers are terminated, DONE is set (RXVES bit 5) and, if enabled, an interrupt is requested. If the word count is greater than the limit for the density specified, the controller asserts WC OVF (RXVES bit 10).



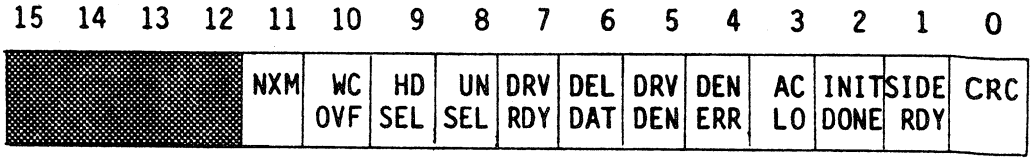
4.3.5 Bus Address Register (RXVBA)

This register is used to generate the bus address, defining the location of data transfer. The register is incremented after each transfer. It will increment across 32K boundary lines via the extended address bits in the Control and Status register. Systems with only 16 address bits will wraparound to location zero when the extended address bits are incremented.



4.3.6 Error and Status Register (RXVES)

This register contains the current error and status conditions of the drive selected by bit 4, Unit Select, of the RXVCS. The RXVES is loaded into the RXVDB upon completion of a function. Read Only.



NXM — NONEXISTENT MEMORY ERROR. This bit is asserted by the controller when the memory address specified for a DMA operation is nonexistent.

WC OVF — WORD COUNT OVERFLOW. This bit indicates that the specified word count is greater than the limit for the density selected. When this error is detected, the control ler terminates the fill or empty buffer operation and asserts the Error and Done bits.

HD SEL — HEAD SELECT. This bit indicates the selected side. Bit cleared = side 0, bit set = side 1.

UN SEL — UNIT SELECT. This bit indicates the selected drive. Bit cleared = drive 0, bit set = drive 1.

DRV RDY — DRIVE READY. This bit is asserted if the selected drive exists with proper power, a diskette is installed and up to speed and the door is closed. This bit is valid when retrieved via a Read Status function or at the completionof INIT, when it indicates the status of drive 0.

DEL DAT — DELETED DATA. This bit indicates that, during data recovery, the identification mark preceding the data field was decoded as a deleted data mark.

DRV DEN — DRIVE DENSITY. This bit indicates the density of the diskette in the selected drive. Bit cleared = single density, bit set = double density.

DEN ERR — DENSITY ERROR. This bit indicates a density error was detected when information was retrieved from the data field of the diskette. A density error occurs when the density selected differs from that of the data field. Upon detecting this error the controller loads the RXVES into the RXVDB and asserts the Error and Done bits.

AC LO — AC LOW. This bit, set by the controller, indicates a power failure.

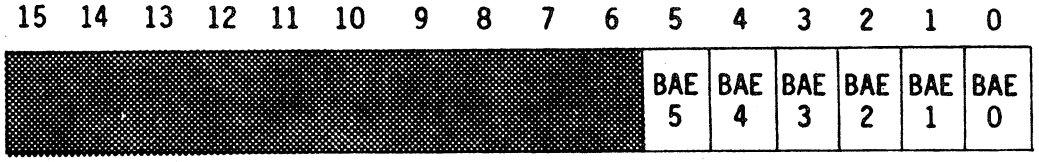
INIT DONE — INITIALIZE DONE. This bit indicates completion of the initialize routine, which can be caused by system power failure or by programmable LSI-11 bus initialize.

SIDE RDY — SIDE READY. This bit is asserted by the controller when double sided drive is selected, is ready, and has double sided media inserted. When asserted, this bit indicates that side 1 of the selected drive is available for Read and Write operations.

CRC — CRC ERROR. This bit indicates a cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. Information stored in the buffer becomes invalid. Upon detection of this error the controller loads the RXVES into the RXVDB and assets the Error and Done bits.

4.3.7 Bus Address Extension Register (RXVBAE)

This register is used to generate the six bus address extension bits in the 22-bit mode. Bit 10 of RXVCS must be written as a one to enable 22-bit mode of operation.



4.4 EXTENDED STATUS REGISTERS

The controller has four internal status registers. These registers provide error information and drive status information. The registers can be retrieved by a read error code function as described in Section 4.5.8.

Word 1 <7:0> - Definitive Error Code

OCTAL	ERROR CODE DESCRIPTION
040	Attempt to access a track greater than 76.
050	Home found before desired track was reached.
070	Desired sector not found after investigating 52 headers (2 revolutions).
120	Preamble not found.
150	Header track address of a good header not comparable with the desired track.
160	Too many tries for an IDAM (identifies header).
170	Data AM not found in alloted time.
200	CRC error on reading the sector from the disk.
240	Density Error
250	Wrong key word for Set Media Density command.
260	Illegal Data AM.
270	Invalid POK during write sequence.
300	Drive not ready.
310	Drive write protected.

Word 1 <15:8> - Not Used

This register is always cleared by the controller.

Word 2 <7:0> - Current Track Address of Drive 0

This register (cleared during INIT to synchronize with actual track position) is updated with each Seek on drive 0 and maintains current track position.

Word 2 <15:8> - Current Track Address of Drive 1

This register (cleared during INIT to synchronize with actual track position) is updated with each Seek on drive 1 and maintains current track position.

Word 3 <7:0> - Target Track of Current Disk Access

If legal, the track specified for the last Read/Write command is saved in this register.

Word 3 <15:0> - Target Sector of Current Disk Access

The sector specified for the last Read/Write command is saved in this register.

Word 4 <15:8> - Track Address of Selected Drive

This register contains the track address read from the sector header of the desired sector during the last Read/Write command.

4.5 COMMAND PROTOCOL

Data storage and recovery using the controller is accomplished by manipulation of the Control and Status (RXVCS) and Data Buffer (RXVDB) registers according to the protocol of the individual functions. The penalty for violation of protocol can be permanent loss of data. Each of the functions are encoded and written into the RXVCS, bits 1-3, as described in Section 4.2. The detailed protocol for each function is described below.

4.5.1 Fill Buffer (000)

This function is used to fill the controller buffer with data from the host CPU. The host specifies the number of words to be transferred. The command density bit determines the buffer size (64 or 128 words). The controller zero-fills the remaining buffer space. If the word count is too large for the density selected, the function is aborted, Error and Done are assetted and the Word Count Overflow bit is set in the RXVES.

The contents of the buffer may be written on the diskette with a subsequent Write Sector command or returned to the host CPU using an Empty Buffer command.

When the command is loaded, RXVCS, bit 5 (Done) is negated. RXVCS, bit 8 (DEN), must be set to define the buffer size. RXVCS, bits 1 and 13 (extended Address) , must also be asserted to define the extended memory segment used with the buffer address yet to be specified, to form the absolute memory address of the data to be transferred. RXVCS, bit 4 (Unit Select) and bit 9 (Head Select), are ignored since no drive operation is required. When RXVCS, bit 7 (Transfer Request), is first asserted, the program must move the word count into the RXVDB, which will negate Transfer Request.

When the controller again asserts Transfer Request, the program must move the buffer address into the RXVDB. The controller then negates Transfer Request, initiates a DMA cycle and transfers the first word from the host to the controller buffer. At the end of the transfer the Word Count register is decremented, and the buffer address is incremented by two. This cycle is repeated until the Word Count register becomes zero. The controller zero-fills the remaining buffer space, sets the Done bit and, if enabled, causes an Interrupt Request. After Done is asserted, the RXVES is moved into the RXVDB.

During the data transaction, if any nonexistent memory is addressed, the controller will time out and abort the function. The Error and Done bits will be asserted, RXVES, bit 11 (NXM), will be set and the RXVES will be moved into the RXVDB. If enabled, an Interrupt Request will be generated.

4.5.2 Empty Buffer (001)

This operation transfers the contents of the controller to the host CPU which specifies the number of words to be transferred. The command density bit determines the maximum legal word count. If the word count specified is too large for the density selected, the function is aborted, Error and Done are asserted, and the Word Count Overflow (WC OVF) is set in the RXVES.

The contents of the buffer may be transferred to the host as many times as desired or may be written on the diskette with a subsequent Write Sector command. Unless a Fill Buffer or Read Sector command is issued, the controller buffer is not destroyed.

When the command is loaded, RXVCS bit 5 (Done) is negated, and bit 8 (Density Select) must be set to allow the proper word count limit. Bits 12 and 13 (Extended Address) must also be asserted to define the extended memory segment used with thebuffer address (yet to be specified) to form the absolute memory destination address. Bit 4 (Unit Select) and bit 9 (Head Select) are ignored since no drive operation is required. When bit 7 (Transfer Request) is first asserted the program moves the word count into the RXVDB, which negates Transfer Request. When Transer Request is again asserted, the program moves the buffer address into the RXVDB. The controller then negates Transfer Request, initiates a DMA and transfers the first word of the buffer to the host. At the end of the transfer the Word Count register is decremented and the Buffer Address register is incremented by two. This cycle is repeated until the Word Count register becomes zero.*

During DMA transactions, if any nonexistent memory is addressed, the controller will time out and abort the function. An Error bit will be asserted.*

*Done is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request is generated at this point.

4.5.3 Write Sector (010)

The Write Sector function locates a desired track and sector and writes the sector with the contents of the internal sector buffer. When RXVCS is loaded with this command, the RXVES is cleared and Transfer Request and Done are negated. When Transfer Request is first asserted, the program loads the desired sector address into the RXVDB, which negates Transfer Request. When Transfer Request is again asserted, the program loads the desired track address into the RXVDB, which negates Transfer Request. The controller then seeks the desired track and sector. The desired track and track field of the sector header are compared. If they do not match, the operation is aborted and Error is asserted.*

If the densities agree, but the desired sector cannot be located within two revolutions, the operation will be aborted and Error will be asserted.*

If the desired track and sector are located and the densities agree, the contents of the internal sector buffer are written followed by a CRC character in the selected density.* Note that the contents of the sector buffer are not destroyed by a Write Sector operation.

CAUTION

The contents of the internal sector buffer are lost during a power failure. However, after power is restored, a Write Sector command will cause the random contents of the buffer to be written on the diskette with a valid CRC character.

4.5.4 Read Sector (011)

This function locates the desired track and sector and transfers the contents of the data field into the internal sector buffer. When the RXVCS is loaded with this command, the RXVES is cleared and the Transfer Request and Done bits are negated. When Transfer Request is first asserted, the program loads the desired sector address into the RXVDB, which will negate Transfer Request. When Transfer Request is again asserted, the program loads the desired track address into the RXVDB, which will negate Transfer Request.

Transfer Request and Done bits remain negated while the desired sector is located. If after two revolutions the desired sector is not located, the operation is aborted and Error is asserted.

*Done is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request is generated at this point.

When the desired sector is located, the desired track and the track field of the sector header are compared. If they do not agree, the operation is aborted and Error is asserted.

If the desired track and sector agree, the data addres mark is read and diskette density is determined. If the diskette density does not compare with the function density, the operation is aborted and Error is asserted.

If a legal data address mark is located and the densities of the diskette and function agree, data from the sector is read into the internal buffer. If the data addres mark indicates a deleted data field, RXVES bit 6 (Delete Data) is set. As data are stored in the internal buffer, a CRC is computed and the CRC bytes are recorded. A non-zero result indicates a Read Error. When a CRC error is encountered, RXVES bit 0 (CRC) is set.*

If the desired sector is located, the density of the diskette and function agree and the data are transferred with no CRC error, Done is asserted and, if enabled, an Interrupt Request is generated.

4.5.5 Set Media Density (100)

This dual purpose function can set media density of "reformat" a diskette. Media density is set by rewriting all the data address marks (single or double density) and writing zero data fiels in the selected density. "Reformatting" the entire diskette is done by writing both the sector headers and the data fields. The data fields are written in the selected density preceded by the corresponding data address mark. Both commands are initiated by the Set Media function but differ in the keyword required to execute the command.

When the RXVCS is loaded with Set Media Density, the RXVES is cleared and Done is negated. When Transfer Reques is set, the program responds with a keyword which must be deposited in the RXVDB to complete the protocol. When the controller recognizes this character, it begins executing the command. If an illegal keyword is used, the operation is aborted.*

If the keyword is 111, a Set Media Density operation is asserted. This operation starts at track 0, sector 1. Each sector header is located and a Write operation is initiated. A data field is written with zero data in the selected density. If an error occurs while reading any header, the operation is aborted.* If the operation is successfully completed, Done is set and, if enabled, the controller asserts an Interrupt Request.

*Error and Done are asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request is generated at this point.

If the keyword is 222, a Format operation is initiated. This function starts at the physical index of track 0. Each track is written first with an index address mark, then 26 sector headers are written sequentially about the track. When each track is written, Set Media Density is set as described above.

The following input string will format the selected unit, in the desired density:

777170	004040	XXX	<LF>
177172	000000	222	<CR>

CAUTION

The Set Media Density operation takes about 15 seconds and the Format operation takes about 45 seconds. Do not interrupt these functions. If either operation is interrupted or an error occurs, an illegal diskette is generated, and the operation must be repeated.

4.5.6 Read Status (101)

This function, initiated by reading the command into the RXVCS, updates the drive status information. Done is negated and RXVES bit 7 (Drive Ready) is updated by sampling the drive ready status line. Drive density is updated by loading the head of the selected drive and reading the first data address mark. This operation requires about 250ms to complete.*

4.5.7 Write Deleted Data Sector (110)

This operation is the same as the Write Sector (010) operation except that the data address mark preceding the data is not the standard data address mark. A single or double density deleted data address mark is written according to the density of the function.

4.5.8 Read Error Code (111)

This function, initiated by loading the RXVCS with the command, retrieves the Extended Status registers. Done is negated. When Transfer Request is asserted the program loads the bus addres into the RXVDB, which negates Transfer Request. Under DMA control one word at a time is assembled and transferred to memory starting at the specified address.

*Done is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request is generated at this point.

If nonexistent memory is encountered during the transfer, the operation is aborted, and Error is asserted.*

When all four words are transfered, Done is set and, if enabled, an Interrupt Request is generated.

4.5.9 Command Protocol for 22-bit Mode

Bit 10 of RXVCS must be written as a one to invoke 22-bit mode of operation.

A change in command protocol applies only to Fill Buffer, Empty Buffer and Read Error Code commands; all other commands remain the same.

For the above commands one more Transfer Request is asserted by the controller to allow loading of the RXVBAE register by the program. After this transfer is completed Transfer Request is negated and the commands proceed as before with the Done bit asserted upon command completion.

*Done is asserted, RXVES is moved into the RXVDB and, if enabled, an Interrupt Request is generated at this point.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

LAST REFERENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U71
CAPACITOR	C37
RESISTOR	R24
RESISTOR MODULE	RU2
TRANSISTOR	Q4
DIODE	CR5
CONNECTOR	J1
OSCILLATOR	Y1

REF. DESIG.	GATES USED PER TOTAL	PART NUMBER
U12	NOT USED	SPARE
U29	2 / 4	74S32

SIDE 2		SIDE 1	
+5V	A	BIRO5L	SOLDER SIDE
	B	BIRG6L	
GND	C	BDAL16L	
	D	BDAL17L	
BDOUTL	E		
BRPLYL	F		
BDINL	H		
BSYNCL	J		
BWTBTL	K		
BIRO4L	L		
BIAKIL	M		
BIAKOL	N	BDMRL	
BBS7L	P		
BDMGIL	R		
BDMGOL	S		
BINITL	T	GND	
BDALOL	U		
BDALIL	V		
+5V	A	BDCOKH	COMPONENT SIDE
	B	BPOKH	
GND	C		
	D		
BDAL2L	E		
BDAL3L	F		
BDAL4L	H		
BDAL5L	J		
BDAL6L	K		
BDAL7L	L		
BDAL8L	M		
BDAL9L	N	BSACKL	
BDAL10L	P	BIRG7L	
BDAL11L	R		
BDAL12L	S		
BDAL13L	T	GND	
BDAL14L	U		
BDAL15L	V		

CONNECTOR A

CONNECTOR B

J1

1	2	1643
3	4	
5	6	
7	8	
9	10	TWO SIDED
11	12	
13	14	SIDE SEL
15	16	
17	18	HEAD LOAD
19	20	INDEX
21	22	READY
23	24	
25	26	DRV SEL 1
27	28	DRV SEL 2
29	30	
31	32	
33	34	DIR
35	36	STEP
37	38	WRITE DATA
39	40	WRITE GATE
41	42	TRACK Ø
43	44	WRT PROT
45	46	RAW
47	48	
49	50	

PRIORITY LEVEL CONFIGURATION

PRIORITY LEVEL	ASSERT LEVEL	MONITOR LEVEL	JUMPER 34/35	34/33	40/41	39/40	31/32	31/30	43/42	43/44	37/38	37/36
4 *	4	5,6	OUT	IN	OUT	IN	IN	OUT	OUT	IN	IN	OUT
5	4,5	6	OUT	IN	IN	OUT	IN	OUT	OUT	IN	OUT	IN
6	4,6	7	IN	OUT	OUT	IN	OUT	IN	IN	OUT	IN	OUT
7	4,6,7	NONE	IN	OUT	IN	OUT	OUT	IN	IN	OUT	OUT	IN

* FACTORY PRESET

ADDRESS	STANDARD	ALTERNATE
DEVICE	177170	177174
VECTOR	264	270

MISCELLANEOUS OPTIONS

OPTION	JUMPERS: DRIVE SELECT 3/2	1/2	SIDE SELECT 6/7	6/5	6/8	WIRE CURRENT 9/10	BOOTSTRAP 26/25	26/27	WRITE PRECOMP 18/19	18/17	FACTORY TEST 15/16	13/14	20/21	11/12	DEVICE READY 47/49	49/48	22 BIT ADDRESS 45/46
BOOTSTRAP ENABLED							IN	OUT			MUST ALWAYS BE OUT	DO NOT REMOVE - FOR TEST ONLY	DO NOT REMOVE - FOR TEST ONLY	DO NOT REMOVE - FOR TEST ONLY			
BOOTSTRAP ** DISABLED							OUT	IN									
WRITE PRECOMP ** ENABLED									IN	OUT							
WRITE PRECOMP DISABLE									OUT	IN							
WRITE CURRENT CONTROL ENABLED						IN											
WRITE CURRENT ** CONTROL DISABLED						OUT											
SINGLE OR DOUBLE ** SIDED DRIVERS	OUT	IN	IN	OUT	OUT												
ONE DOUBLE SIDED DRIVE DRIVE 0 = SIDE 0 DRIVE 1 = SIDE 1	IN	IN	OUT	IN	OUT												
STANDARD READY															OUT	IN	
TRUE READY															IN	OUT	
ENABLE 22 BIT ADDRESSING																	OUT
DISABLE 22 BIT ADDRESSING																	IN

NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
±1/64 .XX ±.020 ±0°30'
.XXX±.010

MATERIAL

FINISH

DO NOT SCALE DRAWING

DRAWN	G.O'Kinsey	12-29-82
CHECKED		
ENGINEER		
APPROVED		
APPROVED		

Sigma Information Systems Inc.

TITLE: SCHEMATIC DIAGRAM — SDC-RXV31, FLOPPY CONTROLLER

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC

SCALE NONE | WORK ORDER NO. | SHEET 1 OF 8

REV NC
SH 1
DWG NO SD400255

Q BUS INTERFACE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

BDAL0 L (4/B-1) TDA0 — AU2 — U16 BUS2 — RDA0 (4/B8)
BDAL1 L (4/B-1) TDA1 — AV2 — U16 IN1 — RDA1 (3/C-8),(4/B-8)
BDAL2 L (4/B-1) TDA2 — BE2 — U16 BUS3 — RDA2 (3/D-8),(4/B-8)
BDAL3 L (4/B-1) TDA3 — BF2 — U16 BUS4 — RDA3 (3/D-8),(4/B-8)
U16: 8641

BDAL4 L (4/B-1) TDA4 — BH2 — U3 BUS2 — RDA4 (3/D8) (4/B8)
BDAL5 L (4/B-1) TDA5 — BJ2 — U3 IN1 — RDA5 (3/D8) (4/B8)
BDAL6 L (4/B-1) TDA6 — BK2 — U3 BUS3 — RDA6 (3/D8) (4/B8)
BDAL7 L (4/B-1) TDA7 — BL2 — U3 BUS4 — RDA7 (3/D8) (4/B8)
(3/D-1) INT ENB — U26 (7438) — U3 ENBA
(3/B-4) SELCSR — U26 (7438) — U3 ENBB
U3: 8641

BDAL8 L (4/B-1) TDA8 — BM2 — U14 BUS2 — RDA8 (3/C-8),(4/B-8)
BDAL9 L (4/B-1) TDA9 — BN2 — U14 IN2 — RDA9 (3/D-8),(4/B-8)
BDAL10 L (4/B-1) TDA10 — BP2 — U14 BUS3 — RDA10 (3/C-8),(4/B-8)
BDAL11 L (4/B-1) TDA11 — BR2 — U14 BUS4 — RDA11 (3/C-8),(4/B-8)
U14: 8641

BDAL12 L (4/A-1) TDA12 — BS2 — U1 BUS2 — RDA12 (3/C-8),(4/B-8)
BDAL13 L (4/A-1) TDA13 — BT2 — U1 IN2 — RDA13 (4/B-8)
BDAL14 L (4/A-1) TDA14 — BU2 — U1 IN3 — RDA14 (3/A-8),(4/A-8)
BDAL15 L (4/A-1) TDA15 — BV2 — U1 BUS4 — RDA15 (4/A-8)
(6/A-1) BUS ENB — 74S04 U36 — U1 ENBA
(6/A-1) TBS7-PRECOMP — U26 (7438) — U1 ENBB — BS7 (2/D-5)
U1: 8641

BDIN L (6/C-1) TDIN — AH2 — U11 BUS3 — RDIN (3/B-3,B-8),(6/C-8)
BDOUT L (6/C-1) TDOUT — AE2 — U11 IN3 — RDOUT (3/B-8),(6/C-8)
BSYNC L (6/C-1) TSYNC — AJ2 — U11 BUS2 — RSYNC (3/C-8),(6/C-8)
BRPLY L (3/C-5) TRPLY — AF2 — U11 IN2 — RRPLY (6/C-8)
U11: 8641

BINIT L — AT2 — U8 — RINIT (3/A-8)
(2/B-6) BS7 — U8 — RBS7
BBS7L — AP2 — U8
BDMGI L — AR2 — U8 — DMGI (3/C-3)
BIAKI L — AM2 — U8 — IAK1 (6/C-8)
R21 180, R18 390, +5V
R17 180, R16 390, +5V
U8: 8640

PU2

(6/C-1) DMR — U10 — AN1 BDMRL
TSACK — U10 — BN1 BSACK L
IRQ — U10 — AL2 BIRQ4 L
TWTBT — U10 — AK2 BWTBTL
U10: 7438

R23 390 — GND
R22 180 — +5V

(6/A-2) EN17L — U9 — AC1 BDALIG L
(4/C-1) A16 — U9
(4/C-1) A17 — U9 — AD1 BDALI7 L
(3/B-1) ENB DMGO — U9 — AS2 BDMGO L
(3/B-1) INT GRANT — U9 — AN2 BIAKO L
U9: 7438

R19 390 — GND
R20 180 — +5V

BDCOK H — BA1 — BDCOK H (8/A-8)
BPOK H — BB1
BIRQ5 L — AA1 — W44 W43 W42
BIRQ7 L — BP1 — W38 W37 W36
BIRQ6 L — AB1 — W32 W31 W30
U7: 8641 — $\overline{DCOK}$ (3/A-8); $\overline{POK}$ (3/A-8),(6/A-8)
W39 W40 W41 W33 W35 W34 — U20 (74S02) — INT PRIORITY (3/B3)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 2 OF 8	

REV. NC — SH. 2 — DWG. NO. SD400255

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

Q BUS CONTROL

(2/D-6) RDA2, RDA3
(2/C-6) RDA4, RDA5, RDA6, RDA7, RDA9
(2/B-6) RDA11
(2/C-6) RDA8
(2/C-6) RDA10, RDA12
(2/C-1) RBS7
93427 U25 — A0 A1 A2 A3 A4 A5 A6 A7 CS1 CS2 — Q0 Q1 Q2 Q3
+5V
1K RU2
U18 74S10
PU2
74LS175 U27 — CLR A B C D CLK — QA QB QC QD
W22 W23 W24 W25 W26 W27
MATCH (6/A-8)
BOOT (6/A-8)
LA01 (6/A-8)
PU1
(2/D-6) RDA1
(2/A-6) RSYNC
(6/C-1) REPLY
U38 74S04
U30 74S00
TRPLY (2/A-8)
(6/C-1) LOG RPLY ENB
U30 74S00
U32 74S08
U18 74S10
(2/A-6) RDIN
(2/A-6) RDOUT
U19 74S86
U31 74S11
SEL CSR (2/C-8)
U31 74S11
STB CSR (3/D-3)
U30 74S00
(2/B-6) RDA14
(2/D-1) RINIT
U38 74S04
(2/B-1) DCOK
(2/B-1) POK
U19 74S86
U20 74S02
U19 74S86
INT (3/B-3,D-3),(4/C-2),(6/C3,C6)

PU1
(2/C-6) RDA6
(3/B-5) STBCSR
U48 74276
INT ENB (2/C-8),(6/C-8)
(3/A-5) INT

PU2
(6/C-1) DMR
U33 74S74
DMGRANT (6/C-8)
(2/D-1) DMGI
U19 74S86
R15 100Ω
C29 820pf
U32 74S08
ENB DMGO (2/A-4)

PU2
(6/C-1) IRQ
(2/B-1) INT PRIOR
U32 74S08
U33 74S74
INT GRANT (6/C-8)
(2/A-6) RDIN
INT GRANT (2/B-4)
(3/A-5) INT

REV. NC
SH 3
DWG NO 5D400255

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 3 OF 8	

FORM NO 002

MUP-8 BIT

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

(5/B-1) BR18
(5/C-1) BR14, BR15
(5/B-1) BR16, BR17
(5/C-1) BR10, BR11, BR12, BR13
(5/A-1) BR22, BR23, BR21
(5/B-1) IDO, ID1, ID2, ID3
PU2
(7/D-1) 6MHz
(6/D-1) WRTRAM, STBBA
(5/C-1) BR9
(5/A-1) SELBUS
(5/D-1) BR7, BR6, BR5, BR4, BR3, BR2, BR1, BRØ

U46 2901 RAM 3 Q3
U47 2901 RAM 3 Q3
U38 74S04
U29 74S32
U26 7438
RU2 +5V 1K
RU12 +5V 1K
U5 74LS174
U6 7438
BF1 BA21L
BE1 BA20L
BD1 BA19L
BC1 BA18L
A17
A16
(6/C-1) TSACK
(3/A-5) INT
U15 TMS4044
RAM DATA (6/A-8)
F=Ø (6/D-8)
7F (6/B-8),(8/C-8)
CARRY (6/B-8)

U13 74LS257
U12 74LS257
U17 74LS396
U4 74LS396
TDAØ, TDA1, TDA2, TDA3 (2/D-8)
TDA8, TDA9 (2/C-8)
TDA10, TDA11 (2/B-8)
TDA4, TDA5, TDA6, TDA7 (2/B-8)
TDA12, TDA13, TDA14, TDA15 (2/C-8)

(2/D-6) RDAØ
(2/C-6) RDA8
(2/D-6) RDA1
(2/C-6) RDA9
(2/D-6) RDA2
(2/B-6) RDA10
(2/D-6) RDA3
(2/B-6) RDA11
(2/C-6) RDA4
(2/B-6) RDA12
(2/C-6) RDA5
(2/B-6) RDA13
(2/C-6) RDA6
(2/B-6) RDA14
(2/C-6) RDA7
(2/B-6) RDA15

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		5D400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 4 OF 8	

DWG NO 5D400255 REV NC SH 4

FORM NO 002

CONTROL ROM & INSTRUCTION DECODE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

(6/C-4) MA0 MA1 MA2 MA3
(6/B-4) MA4 MA5 MA6 MA7
(6/A-4) MA8 MA9
(6/A-4) MA10

82S185 U68 100013-105
82S185 U67 100013-104
82S185 U66 100013-103
82S185 U65 100013-102
82S185 U64 100013-101
82S185 U63 100013-100
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 P/E1 O1 O2 O3 O4
W14
W13

745374 U59
(7/D-1) 6MHz
D0 D1 D2 D3 D4 D5 D6 D7 CPI CS Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
BR0 BR1 BR2 BR3 (4/A-8),(6/C-3)
BR4 BR5 (4/A-8),(6/C-2)
BR6 BR7 (4/A-8),(6/C-8)

R0 R1 R2 R3 (6/C-6)
R4 R5 R6 R7 (6/B-6)
R8 R9 (6/A-6)
R15 (6/D-8)

745374 U57
BR8 (6/C-8)
BR9 (4/B-8)
BR10 BR11 BR12 BR13 (4/D-8)
BR14 (4/D-8),(6/D-5)
BR15 (4/D-8)

745288 U37 Vcc GND +5V
A0 A1 A2 A3 A4 CS Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
ID0 (4/D-8)
ID1 (4/C-8)
ID2 (4/C-8),(8/D-8)
ID3 (4/C-8),(8/D-8)
CC0 CC1 (6/D-3)
BS0 BS1 (6/D-5)

745374 U55
BR16 BR17 BR18 (4/D-8)
BR21 BR22 BR23 (4/D-8)

74S08 U32
74S04 U38
SEL BUS (4/B-8)

R17 R16 (6/D-8)

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 5 OF 8	

REV. NC
SH. 5
DWG NO. SD400255

FORM NO. 002

BRANCH MUX & MICRO SEQUENCER

CONTROL DECODE & CONTROL LATCH

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

+5V — R25 1K — W45 — W46

(7/D-1) 6MHz

(5/C-1) R15

(5/A-1) R16, R17

(4/C-1) F=Ø

(7/B-2) DATA FLG

(7/B-2) SEP DATA, SEP CLK

(2/D-2) IAKI — U18 — (3/B-1) INTGRANT — 74S10

74LS251 U42: A=7/D-1 6MHz; B=5/C-1 R15; C=5/A-1 R16, R17; D0=4/C-1 F=Ø; D1=7/B-2 DATA FLG; D2=7/B-2 SEP DATA; D3=7/B-2 SEP CLK; D4=(2/D-2) IAKI; D5=(3/B-1) INTGRANT; D6=+5V; D7=GND; S=GND; Y=5; W=6

74276 U48: J=9, C=8, K=7, Q=6

74S288 U49: A0=10 (5/B-1 BSØ), A1=11 (5/B-1 BS1), A2=12 (5/C-1 BR14), A3=13, A4=14, CS=15, GND=8, +5V=16; Q0=1, Q1=2, Q2=3, Q3=5, Q4=6, Q5=7, Q6=9, Q7

74LS251 U35: (5/D-1) BR6, BR7; (5/C-1) BR8; (3/D-1) INT ENB; (3/C-1) DMGRANT; (2/A-6) RDOUT, RDIN, RSYNC, RRPLY; Y=5; W=6

74LS251 U34: R14 1K — J1-10 — W16 — W15; (8/A-1) INDEX, READY, TRACKO, WRT PROTECT; (7/C-1) RDATA; (4/C-1) 7F; (4/C-1) CARRY; Y=5; W=6

74LS251 U36: +5V — 1K RP12 — ALT VECTOR — W28 — W29; (3/D-5) MATCH, BOOT; (3/C-5) LAOI; (2/B-1) POR; (8/B-3) CRC ERR; (8/C-3) CRC DATA; (4/C-1) RAM DATA; Y=5; W=6

2911 U60: (7/D-1) 6MHz; (5/D-1) RØ, R1; (5/C-1) R2, R3; (3/A-5) INT; W12 W11; Y0=12 MAØ, Y1=13 MA1, Y2=14 MA2, Y3=15 MA3 (5/D-8)

2911 U58: (5/C-1) R4, R5, R6, R7; Y0=12 MA4, Y1=13 MA5, Y2=14 MA6, Y3=15 MA7 (5/D-8)

2911 U56: (5/C-1) R8, R9; Y0=12 MA8, Y1=13 MA9, Y2=14 MA10 (5/D-8)

74S139 U44: (5/B-1) CCØ, CC1; (7/D-1) E6MHz; Y0=12 WRT RAM (4/C-8),(8/B-8); Y1=11 STB BA (4/C-8); Y2=10; Y3=9

74S139 U44: (5/D-1) BR4, BR5; Y0=4; Y1=5; Y2=6; Y3=7

74259 U22: (5/D-1) BR1, BR2, BR3, BRØ; (3/A-5) INT; Q0=4 TSYNC, Q1=5 TDOUT, Q2=6 TDIN (3/A-8); Q3=7 REPLY (3/C-8); Q4=9 TWTBT (2/C-4); Q5=10 IRQ (2/C-4),(3/B-3); Q6=11 DMR (2/C-4),(3/C-3); Q7=12 TSACK (2/C-4),(4/D-3)

74259 U23: Q0=4 LOG RPLY ENB (3/B-8); Q1=5 ENB CRC (8/C-8); Q2=6 CALC CRC (8/B-8); Q3=7 MFM (7/C-8),(8/C-8); Q4=9 VCO SYNC (7/C-8); Q5=10 DATA FLG ENB (7/A-8); Q6=11 HOLD PLL (7/A-8); Q7=12 WRITE GATE (8/A-8,D-8)

74259 U24: Q0=4 DRIVE SEL 1 (8/B-8); Q1=5 DRIVE SEL 2 (8/A-8); Q2=6 HEAD LOAD, Q3=7 SIDE SEL (8/B-8); Q4=9 DIRECTION (8/A-8); Q5=10 STEP (8/A-8); Q6=11 TBS7-PRECOMP (2/B-8),(8/B8,C8); Q7=12 BUS ENB (2/B-8)

74259 U21: Q0=4; Q1=5; Q2=6; Q3=7 EN17 L (2/C-5); Q4=9; Q5=10; Q6=11; Q7=12

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 6 OF 8	

DWG. NO. SD400255 REV. 8

FORM NO. 002

DATA SEPERATION & MASTER TIMING

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

(8/A-1) RAW
(6/B-1) VCO SYNC
MFM
(3/A-5) INT
(6/B-1) HOLD PLL
(6/B-1) DATA FLG ENB

E6MHz (6/D-2)
6MHz (6/D-8),(8/C-8)
6 MHz (4/C8),(5/D-4),(6/C-6)
RDATA (6/B-8)
PL CLK (8/C-8)
SEP DATA (6/D-8)
SEP CLK (6/D-8)
DATA FLAG (6/D-8),(8/C-8)

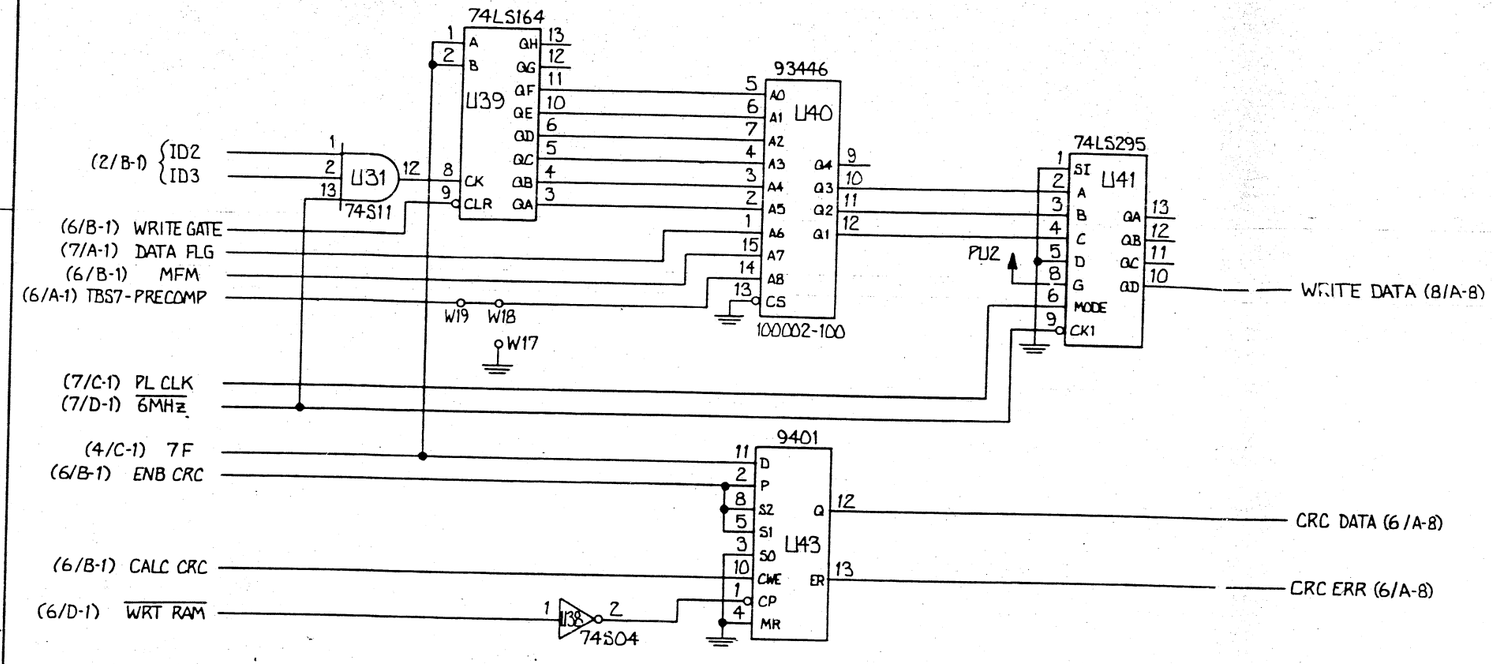
SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 7 OF 8	

DWG NO SD400255 REV NC SH 7

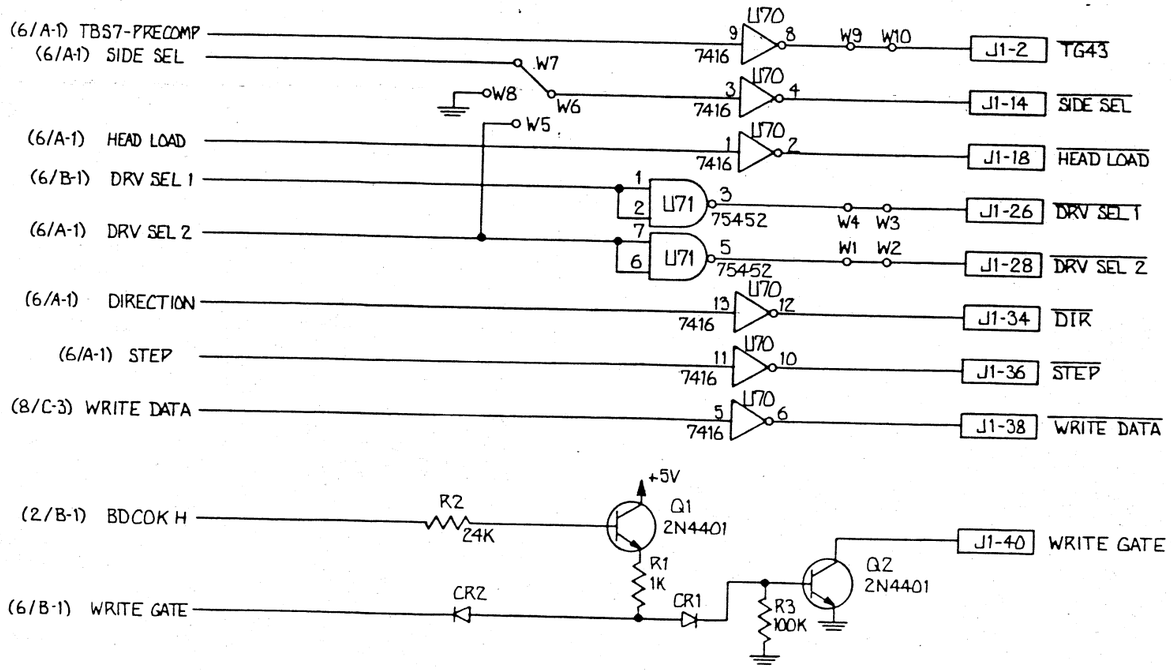
FORM NO 002

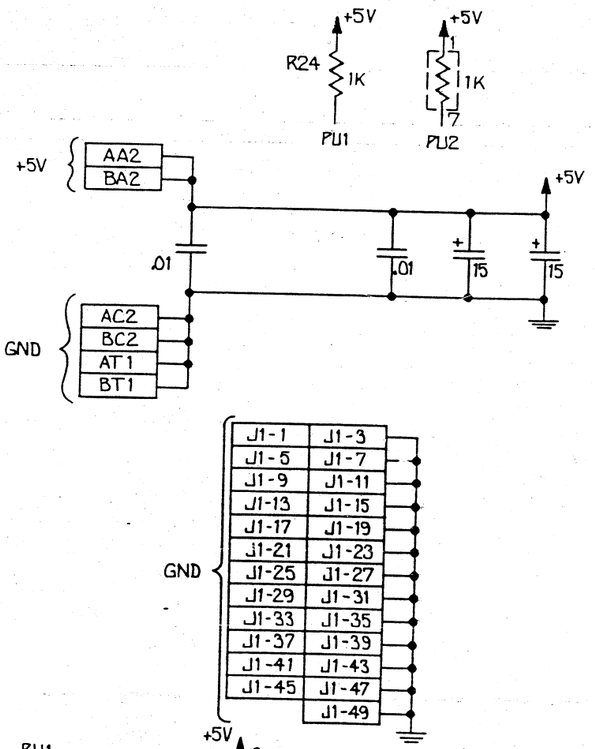
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

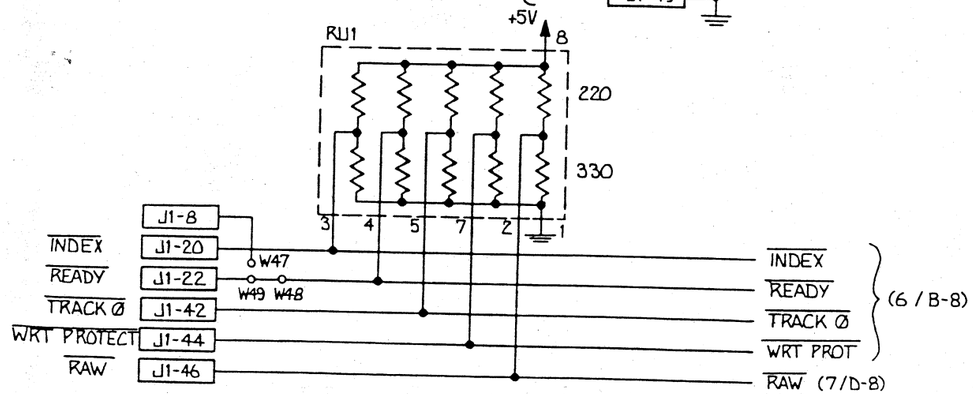
WRITE PRECOMP & CRC GENERATOR



DRIVE INTERFACE







SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400255	NC
SCALE NONE	WORK ORDER NO.	SHEET 8 OF 8	

REV. NC
SH. 8
DWG. NO. SD400255

FORM NO. 902